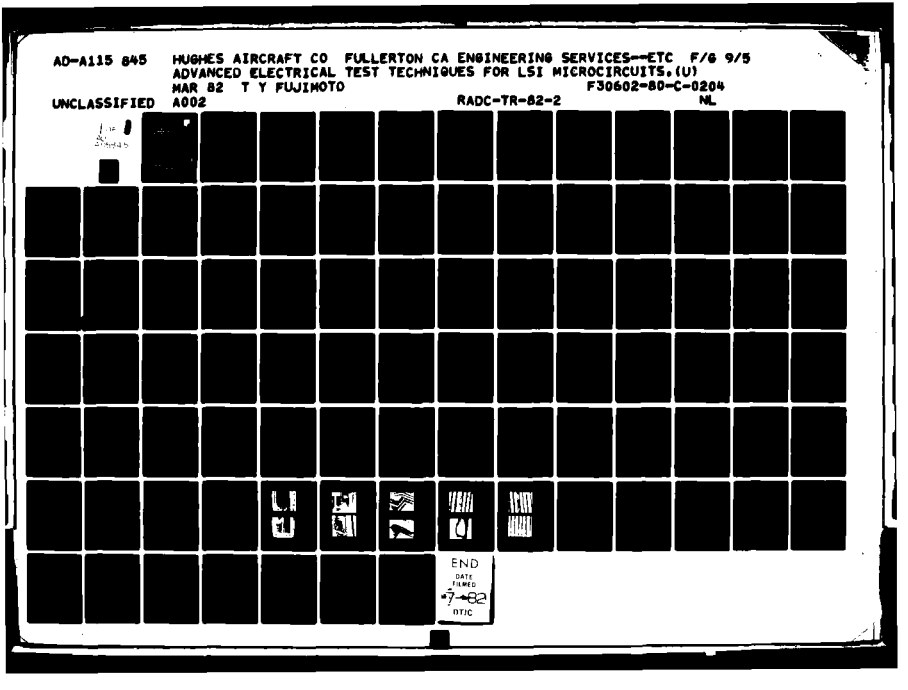
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# ADVANCED ELECTRICAL TEST TECHNIQUES FOR LSI MICROCIRCUITS

Hughes Aircraft Company

Ted Y. Fujimoto





ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

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An investigation was conducted to determine the feasibility of developing new LSI test techniques using test parameters that could be directly related to the physical structure of the device. In addition, a test technique capable of detecting potential failures or increasing safe operating margins was highly desirable. Two test methods were developed and evaluated for static RAMs: (1) Flip flop cell unbalance detection and (2) time-dependent failure detection. Three test techniques were evalu-

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ated for dynamic RAMs: (1) chip enable pulse width, (2) V-BUMP, and (3) refresh time.

The memory cell flip flop unbalance parameter did not correlate with any device degradation or failure under life test conditions. However the unbalance detection technique was found to be useful in detecting functionally tested time-dependent failures.

The chip enable high test with a maximum pulse width, as well as with a minimum pulse width, was determined to be highly useful in evaluating the drive capability margin of the clocked dynamic circuits. The V-BUMP test for checking the sense amplifier's ability to discriminate between "0"s and "1"s in the memory cell was determined to be a highly effective safe-margin testing technique. It was found that refresh time tests at room temperatures are ineffective in screening marginal parts, therefore such tests should be accomplished at high ambient temperatures. None of the three test parameters for dynamic RAMs was able to be correlated with degradation or life test failure. These test techniques were determined to be effective for electrical screening tests and should be included in MIL-M-38510 specifications.

## EVALUATION

Microcircuit electrical testing has evolved from SSI/MSI where parametric measurements were able to monitor device quality based on semiconductor physical properties to the present day situation that exists with respect to testing complex LSI/VLSI devices where the sensitive parametric tests can only access a very small percentage of the chip's active elements available at the input/output pins. The trend has been to completely abandon much of the information that reflects semiconductor quality since it has been assumed that this type of information is not readily available on LSI/VLSI complexity devices. Electrical testing of complex microcircuits has historically been based on "brute force" pattern testing to some arbitrary criterion such as stuck-at-one, stuck-at-zero nodal verification, or in some instances just a quick check of device functionality. The result is usually a go-no-go indication of part performance, typically at nominal signal timing and supply voltage. Since most of the internal circuitry in complex microcircuits is not directly accessible from external pins, there is usually no attempt made to measure sensitive performance characteristics of internal structures such as component leakage currents except as they combine to contribute to a gross measurement such as supply current.

The goal of this study was to develop and evaluate measurements which could be made using only the external pins of present complex microcircuits which would reflect quality (based on semiconductor physics) of internal device structures (gates, transistors, surface, etc). These tests if proven and added to or used to replace existing MIL-M-38510 slash sheet electrical tests, could result in a more reliable product at a potentially lower testing cost, especially in the case of large memories where conventional pattern testing is becoming very time consuming. Manufacturers therefore attempt to use only very minimal and simple patterns. The current objective is to develop test techniques based on this concept to supplement existing electrical tests. These additional tests should be able to detect the small number of unreliable devices not screened by conventional tests and thus provide an increase in the ultimate reliability of critical systems. A long term objective is to develop these test procedures into efficient and comprehensive testing to replace some of the present time consuming electrical tests.

The concept involved in the proposed technique is not new, only the application of the concept to specification testing of complex microcircuits is new. Variations of the concept have been used in the past for system level testing of computer modules such as core memories and in the process characterization testing of microcircuits. The application of this concept, however has not been evaluated as to its potential value as a specification electrical test procedure. This technique requires the identification of internal characteristics related to localized chip quality and capable of being measured using the available external pins. These characteristics should be measureable on as many different internal chip locations as possible. For semiconductor memories, individual cell access time, refresh time, minimum data retention voltage, etc. represent such externally measurable parameters related to specific different internal locations. This study attempted to define some of these potential

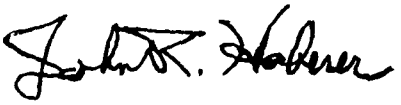
'inferred' measurements and to assess their value as indicators of later life reliability problems.

For the limited number of inferred measurement techniques studied in this effort and with the specific approach used to identify potential correlation it was not possible to draw any conclusions regarding the value of these inferred electrical measurement techniques as specification tests. Many additional techniques could have been developed and evaluated but this was not within the scope of this effort. This study intended to select three different groups of each device representative of initially good, marginal and poor electrical specification performance characteristics and then correlate long term reliability/degradation with initial values of the inferred measurements. Initial screening of large quantities of devices was unable to identify sufficient numbers of marginal/poor devices to meet original requirements. This was due mainly to the fact that all selection was from devices which were procurred to 100 per cent electrical test screening. With sample sizes of five devices in each evaluation group and with expected defect rate of less than 1 percent in these prescreened devices, it was very unlikely that any of the devices being studied would have a problem able to be detected by any of the tests that were evaluated. This is supported by the lack of any relevant failures over the duration of the accelerated life test. Since no relevant failures were observed, it was impossible to correlate the inferred measurement data with any detectable failure mechanisms. Therefore, this study was unable to draw any valid conclusions as to the usefulness of the studied electrical test techniques as indicators of internal chip quality.

One of the most important observations of this study was related to the identification of two devices which were initial failures to the time delay failure test. This is a test which attempts to ensure that a static RAM is really static. Normal specification testing requires that read/write operations be performed at high clock rates and thus a memory cell is verified a very short time after it has been written. Verification is normally nanoseconds to milliseconds after write depending on memory size and organization. In this study, one of the non-standard tests performed was write, wait five seconds, verify. Two devices which passed all specification requirements did fail this test. Unfortunately, due to the five second wait time, this is not a practical 100 percent screen test. However, the evidence indicates that all product should be screened for this problem. The failure mechanism is usually an open or excessively high resistance path that results in a static memory behaving as if it were dynamic. This finding supports work at RADC where some CMOS RAMS were found to have similar characteristics. Others have also observed similar problems as discussed in this report. The existance of this problem points out the need that a test technique be developed as a 100 percent screen test which is fast enough to be used as a specification test and able to verify that all memory locations are indeed static. This study has identified a potential correlation between a test designed to be sensitive to memory cell unbalance (and which can be performed quickly) and the problem of time delay failures in static RAMS which cannot be efficently detected by the write-wait-verify procedure as discussed above. Since no attempt was made to identify the specific mechanisms involved in the time delay failures and since a statistically significant number of devices were not observed, further work must be done to assess the value of the

cell unbalance test in detecting time delay failures. Although this effort only looked to five seconds for time delay failures, there is also concern that some static RAMS may fail after delays considerably in excess of this value. These types of failures are presently not found until board level testing or even worse, not found until some system application requires long static retention times.

The current objective of this study was not achieved in that no specific externally measureable characteristics were identified as sensitive indicators of internal structure quality. This effort did, however provide some insight into the problems associated with obtaining adequate correlation between newly developed electrical test techniques for complex microcircuits and their value as quality indicators and/or reliability predictors. Although not a direct objective of this effort, several existing Mil-M-38510 slash sheet electrical test requirements were identified for improvement. As microelectronic devices increase in complexity it is even more important that electrical test techniques be developed which maximize the amount of information that can be derived from testing. This will ensure the maximum confidence that a device will perform reliabily in its end application. Non-conventional test techniques as addressed in this preliminary study are one way of achieving this goal, and the only way to enhance test confidence with present generation devices. Next generation devices will be designed to be more testable and will make use of various forms of built-in test circuitry to enhance test coverage and confidence. Non-standard test techniques developed as a result of efforts such as this will provide a data base to enable the more efficient implementation of these next generation VLSI/VHSIC designs.



JOHN R. HABERER
Project Engineer

## PREFACE

The test and evaluation program described in this report was performed by the Components Department of the Ground Systems Group of the Hughes Aircraft Company, Fullerton, California, during the period between June 1980 and June 1981. The work was performed for the USAF Rome Air Development Center under contract number F30602-80-C-0204. John R. Haberer of the RADC Reliability Physics Section provided the technical direction.

Key personnel from Hughes contributing to the program were Jim E. Thomas Program Director, Ted Y. Fujimoto Technical Director, Mark I. Growe and Gordon P. Chin of the Sentry ATE Engineering group.

CONTENTS

# SECTION 1
# SUMMARY

## 1. PROGRAM BACKGROUND AND OBJECTIVES

An investigation was undertaken to develop LSI test techniques that would, by means of externally measurable characteristics, relate to the device's in- internal structure quality and be useful as a reliability assessment tool. The memory devices selected as test vehicles (static and dynamic RAMs) represent two mature LSI technologies.

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Often today's parametric testing of complex LSI microcircuits can only access a small percentage of a chip's active elements at the input/output pins. Measurements of internal physical qualities have been bypassed in favor of go/no-go logic and functional testing procedures. Since most of the internal circuitry in LSI microcircuits is not directly accessible from external pins, there is usually no attempt made to measure sensitive performance characteristics of internal structures. Historically, when devices were simple, direct physical measurements of active elements of transistors or diodes, such as gain, capacitance, leakage or voltage breakdown could be made. Such physical parameters have a direct effect on circuit performance, and therefore, are quite useful in predicting ultimate performance, and to some extent, reliability. Thus, it is desirable that such measurements be capable (either directly or indirectly) of being made on current, more complex devices.

It was the intent of this investigation to establish selected and externally measurable LSI electrical characteristics related to the internal strucural characteristics of the device that would be indicators of ultimate device reliability. The selected characteristics were to be a measure of a maximum number of chip locations, using only the available external pins. All internal locations were measured by external means for the identified characteristics and plots made showing the value of the measured characteristics. Any abnormal characteristic physical distribution was investigated to see if it correlated with any future reliability problems. After the measurable characteristics were selected, an evaluation to determine the effectiveness of the associated test procedures was made, and the feasibility of including them in MIL-M-38510 was investigated.

Selection of Test Vehicles - RADC has indicated that to evaluate any new test techniques, at least two mature LSI technologies should be represented by the test vehicles. The requirement to check as much of the chip area as possible narrowed the test vehicle selections to a well-ordered, structured device such as semiconductor memories. Another basic requirement limited the choices to those devices that were readily available at Hughes in the large quantities required to identify a sufficient number of potentially unreliable parts for use as test vehicles. Hughes selected a 2147 static RAM (4Kx1) and 4050/9050 dynamic RAM (4Kx1) as test vehicles, both of which meet all of the requirements.

RAMs have a well-structured chip organization that was suitable for the planned investigation. These devices have over 4000 memory cells plus the periphery circuits, and are well covered by the existing MIL-M-38510 slash sheet specification. The 2147 static RAM is covered by the newly issued slash 238 specification, while the 4050/9050 dynamic RAMs are covered by slash sheet 235A.

2147 Static RAM - This memory, whose basic cell is a flip flop, is the first of a family of high-speed static MOS memories that is starting to compete with the bipolar RAMs, but at a much lower power level.

Introduced by Intel, they are the initial run of the first MOS devices to utilize scaled-down device dimensions to attain higher speed and lower

power without changing technology, but based on standard, proven semiconductor processes. Intersil, Hughes' second source for this device, identifies it as part number 7147.

4050/9050 Dynamic RAM – TI introduced these MOS memories originally with AMD becoming a second source. The basic memory cell is a single capacitor that is accessed by one transistor. There are three supply voltages: $V_{dd}$, $V_{cc}$, $V_{bb}$. $V_{dd}$, at +12 volts nominal, is the main supply voltage. $V_{cc}$, at +5 volts, is only used for TTL compatibility. $V_{bb}$ is used on the chip substrate primarily to reduce physical parameter characteristics such as MOS transistor body effect and parasitic junction capacitances.

TABLE 1. SUMMARY OF OBJECTIVES AND ACCOMPLISHMENTS

| Objective | Accomplishment |
|---|---|
| Investigate the basic memory circuits and test concepts, and identify new possible test methods for incorporation in the study program. | • Literature search, vendor contacts, and talks with key industry technical persons were conducted.<br>• Two test concepts for static RAMs and three test concepts for dynamic RAMs were identified, evaluated, and selected. |
| Select and acquire test vehicles. | • Hughes in-house memory usage was surveyed and the 2147/7147 static RAM, 9050/4050 dynamic RAM were selected. |
| Implement special test parameters and integrate into MIL-M-38510 electrical tests on ATE | • Existing Sentry test programs for test vehicles were modified to add new test concepts. Vmin and TDF for 2147; TREF, TWCE and V-BUMP for 9050. |
| Perform MIL-M-38510 type electrical tests and the special electrical test parameters | • Over 7000 static RAMs and over 5000 dynamic RAMs were tested with standard and special tests to select test vehicles. |
| Select method of presentation of results | • Special test parameters were investigated and results presented using shmoo plots, memory cell maps of cell status, and statistical presentation of data as a function of life test time. |
| Determine significance of special test measurements results | • Significance of test results from initial testing to stressed-life testing is presented in Section 3. |
| Perform 125°C, static bias life tests for 1000 hours | • Life testing was performed on both types of selected test vehicles. |
| Perform statistical analysis on life test electrical measurements. | • Statistical analysis on life test data was performed on the Sentry 610 computer. In particular, average, variance, and data distribution plots were completed. |
| Ascertain degree of success | • Selected test parameters were more directly related to physical characteristics of the device.<br>• Time-dependent failure tests (TDF and Chip Enable Pulse Width) were successful for use in screening devices.<br>• The study of topological distributions of specific electrical measurements did not successfully predict failures. |

## 2. OVERVIEW OF THE STUDY RESULTS

For the static RAMs, the FF cell unbalance parameter was determined to be stable after life tests, while functional tests that were time-dependent failures were found to be detectable using the cell unbalance test techniques. New test techniques for dynamic RAMs were found to be excellent as screening tools, but since the test parameters did not deteriorate or fail under life test conditions, they were not useful as reliability prediction tools.

An investigation was launched to select some externally measurable characteristic related to a chip's internal structure quality and capable of being used for a reliability assessment tool. This characteristic was required to measure as many different chip locations as possible so that abnormalities associated with geographical locations might be linked to potential failure problems. LSI RAMs were considered to be the best choice for a general test vehicle. There are two types of RAMs, static and dynamic, both of which were utilized for this investigation.

This type of investigation requires samples that are readily available in large supply.

The 2147/7147 static RAMs and the 9050/4050 dynamic RAMs are used in large quantity at Hughes Aircraft Company, Fullerton, so these devices were chosen for the primary test vehicles. The 2147 is a 4KX1 fully static RAM available in quantity from both Intel and Intersil. The 9050, equivalent to the 4050, is a 4KX1 dynamic RAM available from American Micro Devices (AMD), and the 4050 is from Texas Instruments (TI).

Static Memories – After extensive investigation, the static memory cell flip-flop (FF) unbalance was selected as one of the primary internal parameters to be studied. An external measurement technique for characterization of this parameter was developed using a memory cell map to record individual memory cell unbalance states as a function of the chip supply voltage. A detailed explanation of this detection algorithm is contained in Section 2.A.

Since an electrically well-balanced FF is dependent upon a physically well-matched layout of both halves of the FF, the main contributions to the unbalance are random defects in the physical structure. Defects can be poor internal contacts from one layer of conductor to another, process contamination, threshold mismatch between FF transistors, excess leakage of the FF transistors, mask misalignment, etc. This cell unbalance can be stable or unstable depending upon the cause. Thus, extensive life testing was necessary to determine the reliability or degradation of these selected devices.

Another test technique that was investigated was the functionally tested time-dependent failure (TDF). It was successful in detecting latent failures and it is recommended as a device qualification or periodic sampling test. Since time intervals up to 5 seconds are necessary, it may not be generally applicable for 100% screening and receiving tests. However, it has been determined that these TDF's can also be detected by the FF cell unbalance test. In particular, if a high test temperature environment is used, the cell unbalance test detects failures in a normal test time mode.

The screening process to find candidates with an anomaly in the test measurements resulted in the number of actual devices found being much less than originally expected. The original plan was to run life tests with 100 selected parts of each type for 1000 hours at 125°C. In order to achieve equivalent time-temperature device hours with the smaller number of sample

devices, two extra steps were taken. The first was to institute a temperature step stress test program to determine the best temperature stress to utilize for the suspected parts. After the proper temperature stress was determined, the time regression chart, of MIL-STD-883, Method 1015.2 was utilized to determine the equivalent time period needed at the new temperature for the number of suspect devices tested. It was determined that for the 30 devices available, a temperature stress of 200°C at a life test of 500 hours was required.

Dynamic Memories – For the dynamic RAMs, three device parameters were selected for investigation: (1) memory cell refresh time TREF, (2) chip enable precharge and active time TWCEL and TWCEH, and (3) memory cell charge margin V-BUMP.

Normally refresh time is an indirect measurement of the worst-case memory cell charge leakage rate. Since leakage rate varies greatly with temperature as well as from one device to another, a fairly large margin between the specification limit and the mean exists. The large variation exists because the capacitor charge leakage is highly dependent upon temperature, process operations, defects, contaminations, and access transistor leakage. In addition, the leakage factor is largely exponential as a function of temperature, since part of the capacitor is a reversed-bias semiconductor diode. In a directly related manner, the TWCEH pulse at the maximum width is also a measure of the leakage rate of the dynamic amplifier bootstrap nodes. These bootstrap nodes must maintain a proper high voltage to allow the bootstrap amplifiers to operate properly. Section 2.B explains in detail how these circuits operate.

TABLE 2. KEY DECISIONS AND FINDINGS

STATIC RAMs

- An FF cell unbalance test technique was selected and developed
- A functional time-dependent failure test was developed and investigated
- Functionally tested time-dependent failures were also found to be detectable with the FF cell unbalance test
- Cell unbalance parameter did not develop into a failure problem when life tests were run

DYNAMIC RAMs

- Refresh time measurements at room temperature do not always screen out failures that may be encountered at high temperatures
- Anomalies in the refresh time test parameter did not develop into failures when life tests were implemented
- TWCEH at its maximum allowable width became an excellent test to check the drive sustaining capability of dynamic circuits
- TWCEL at its minimum allowable width checks the precharge capability of the dynamic circuits
- Correlation of test parameters TWCE, V-BUMP and TREF to device failure was indeterminate, since no failures occurred during life tests.

## 2. OVERVIEW OF THE STUDY RESULTS (Continued)

Early in the program, over 5000 devices for the dynamic RAMS and 7000 for the static RAMs were screened using these test parameters. However, only 18 suspected or marginal parts were identified for each part type. The small number of suspect parts are probably due to the fact that both part types were purchased to MIL-M-38510 class B level quality and thus received MIL type factory screening, burn in, and inspection procedures Therefore, an accelerated stress life test program was formulated and the suspect parts, along with an equal number of non-suspect parts used as references were placed in the life test program. The selected test parameters, as well as the standard test parameters, were monitored carefully to determine if selected test parameters had contributed or were directly related to any device failures. In this case, the life test time, using time temperature regression methods, was established at 1500 hours at 150°C for the dynamic RAMs, and 500 hours for the static RAMs at 200°C.

Analysis of the life test results for the 2147 static RAMs indicates that the failures that occurred were not related to the memory cell FF unbalance. The primary failure was due to electromigration of the metal lines, a completely different mechanism than what the special test was sensitive to. Thus no conclusion can be drawn as to the value of the special test since no legimate failures were seen.

A review of the life test data for the dynamic RAMs indicates that no additional failures or rejects occurred other than those that were determined before the start of the life test program.

No clear statistical method could be gleaned from the cell mapping data for determining failure trends. There were clear indications that TWCEH was greatly affected by variations in TWCEL so that the special test conditions for the chip enable pulse width tests must be well defined.

## SECTION 2
## ANALYSIS OF TEST PARAMETERS AND METHODS

Subsection A – Static RAMs



Subsection B – Dynamic RAMs

## 1. SELECTION OF TEST CONCEPTS

A number of test concepts were reviewed and considered for use in developing special test techniques for LSI microcircuits. The choice of test approaches was narrowed to two: a flip-flop cell unbalance test and a time-dependent test.

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Static RAMs require no refresh time, do not need external clocks, and now have only one supply voltage. Their simplicity does not present very many opportunities to achieve new test techniques.

Table 3 shows the main test concepts that were considered and investigated for this study. A basic electrical parameter that was studied, selected, and used in a test concept was the memory cell flip-flop (FF) unbalance. The primary features of this electrical parameter are: (1) the cells cover the majority of the chip area and are all accessible; (2) a cell margin status between good and bad devices is available; (3) effects can be attributable to physical phenomena such as excessive transistor leakage, back bias diode leakage, or process contaminations; (4) tests can be relatively fast since a single, preselected $V_{CC}$ value can be used as a test parameter screen; and (5) standard test patterns, such as the checkerboard, can be run. In addition to memory cell unbalance tests, time-dependent failure (TDF) tests are available as screening tools, but are normally not acceptable for high speed test requirements, although they can be used for device electrical characterization. Time-dependent tests have been reported previously by others and such delayed failures were induced using accelerated methods.

During the investigation of failures of devices that occurred during time-dependent tests, it was determined that these failure modes can be detected by the cell unbalance tests, and therefore can be considered a special case of cell unbalance failure. In addition, cell unbalance detection methods can be utilized with standard checkerboard test patterns.

Another general area of test concepts is called memory pattern testing. Special test pattern sequences are input to the memory to determine a memory cell's susceptibility to disturbances. However, these test patterns are deterministic and memory designers usually understand their device's weakness to certain patterns as a result of detailed knowledge of the cell physical layout. Such information is available from suppliers or from memory characterization by the user when doing qualification testing. In addition, exotic test patterns, such as Ping Pong, Galpat, and Galwrec, are not always necessary, because cell-to-cell disturbances are not as critical as in the dynamic RAM cells where stored charges are at the mercy of nearby capacitive coupling disturbances.

During memory pattern testing FF cells are latched in stable electrical states and present designs (2147) feature depletion-mode FETS as load resistors, with latched-on transistors conducting typically 1 microampere. However, the newer 16K and some 8K static RAMs feature high resistance polysilicon load resistors stacked in the "Z" direction for higher packing density. Featuring resistors typically in the gigaohm range, these high impedances and the resulting low transistor latching currents could mean nearby cell disturbances and susceptibility to node leakages, which were not problems previously.

An electrical parameter that was also investigated was access time as a function of memory cell location. Although memory cell mapping can be achieved, access time would really be dominated more by address

decoding speed rather than cell speed. After the address is decoded and the proper X and Y lines are defined, then actual speed of the address voltage traveling down the X and Y lines is predictable, and does not vary much within the metal or diffused line grouping, and is relatively fast. Line speed is primarily dependent upon the RC time constant of the metal or diffused lines, and distance of the selected cell from the decoders. It was felt that abnormalities and defects in the address lines can be easily caught in standard high speed memory matrix access time measurements.

Some form of overvoltage stress tests was considered in conjunction with some of the other tests. An overvoltage screen is used by some manufacturers to weed out potential failures. It is a fast test and covers most of the chip area, but it can not be used as a measuring tool for characterization, and the failures are destructive. It was felt that a destructive type screen was not appropriate for this program wherein thousands of parts are being purchased and would be tested. Any high voltage screen test beyond the maximum specification level (typically 150% of normal voltage) may destroy too many parts and was not included within the scope of this investigation.

In essence there were two types of special tests run during initial screening of 2147/7147 devices to find suspect parts. One test screened for excessive memory cell FF unbalance (Vmin), and the other tested for time-dependent failures (TDFs).

TABLE 3. TEST CONCEPT SUMMARY

| Test Concept | Advantages | Disadvantages |
|---|---|---|
| FF Cell Unbalance | • Covers majority of chip area (memory cells)<br>• Marginal status of cells obtainable<br>• Defects relatable to semiconductor physics<br>• Relatively fast<br>• Standard checkerboard pattern-access time | • Life test indicates unbalance parameters do not deteriorate |
| Time-dependent Failure (TDF) | • Covers all circuits on chip<br>• Special case of FF cell unbalance<br>• Can be detected with cell unbalance test at high temperature<br>• Standard checkerboard test pattern time | • Test time is long (up to 5 seconds) |
| Pattern Testing | • Covers all memory cells<br>• Deterministic patterns<br>• Excellent memory cells status and noise check | • Some test patterns are too long<br>• Complex patterns unnecessarily used |
| Access Time | • Can access all memory cells<br>• Memory cell map of speed obtainable<br>• Fast | • Not relatable to semiconductor physics<br>• Gross speed related to address decoder only<br>• Already standard AC parameter test |
| Voltage Stress | • Affects most circuits<br>• Effective as a manufacturing screen<br>• Fast<br>• Standard checkerboard pattern-access time | • Cannot be quantized for characterization<br>• Tends to be destructive if overvoltage is used |

## 2. ANALYSIS OF CELL UNBALANCE TEST CONCEPT

Static RAM flip-flop (FF) cells, while relatively stable circuits and generally reliable, are susceptible to failures resulting from extreme electrical unbalance between the two symmetrical halves of the FF. In addition, faulty I/O lines extending from the FF cell to the output buffer can also modify the cell information, though these effects can be differentiated as a distinct pattern observation in a memory cell map visual display.

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Initial studies of the static 2147 RAMs show that these memories, unlike dynamic RAMs, are less failure prone, or conversely, more reliable (Reference 1). The primary reason for this is that the basic memory cell is a cross-coupled flip flop (FF) that keeps the cell in a relatively stable state by use of its internal feedback network. Additionally, its peripheral circuits are static. Since the true or false state of the FF is the basic memory cell information, the FF will always be in a stable state, except during the transition time. Conversely, the basic design of a dynamic RAM cell requires a charged capacitor to indicate "1" data and a discharged capacitor "0" data. Since the charge on a semiconductor capacitor slowly leaks off, the capacitor must be recharged periodically. Accordingly the very act of recharging a leaky capacitor tends to make the dynamic RAM more susceptible to reliability problems than the static FF cell.

Since the static FF cell RAM is a more stable device, it is more difficult to find new test procedures to explore its weaknesses or defects.

As is true of most semiconductor memories, the major portion of the RAM chip is taken up by the memory cells. These memory cells are made up of FF circuits to obtain speed and reliability. Failure of a FF cell is evidenced by its inability to change state (i.e., stuck at "1" or "0"). Such failures are the result of extreme electrical unbalance between the two halves of the flip-flops.

The 2147 static RAM cell is made up of a six-transistor FF and a corresponding physical layout as shown in Figure 1. In all FF cell designs, it is extremely important that the physical balance between both halves of the FF be as close to perfect as practicable. In other words, a cell must not favor either the "1" state or the "0" state. From a design standpoint this well-balanced state can be attained by careful FF physical layout and matching of FET electrical characteristics. However, random process contamination defects, mask misalignment, or poor contacts can upset the electrical balance. Most of such defective FF cells can be found by normal testing, screening techniques, and burn-in procedures. But for the marginal cases, an unbalance test is needed to detect the potential failures that cannot be revealed by conventional test techniques.

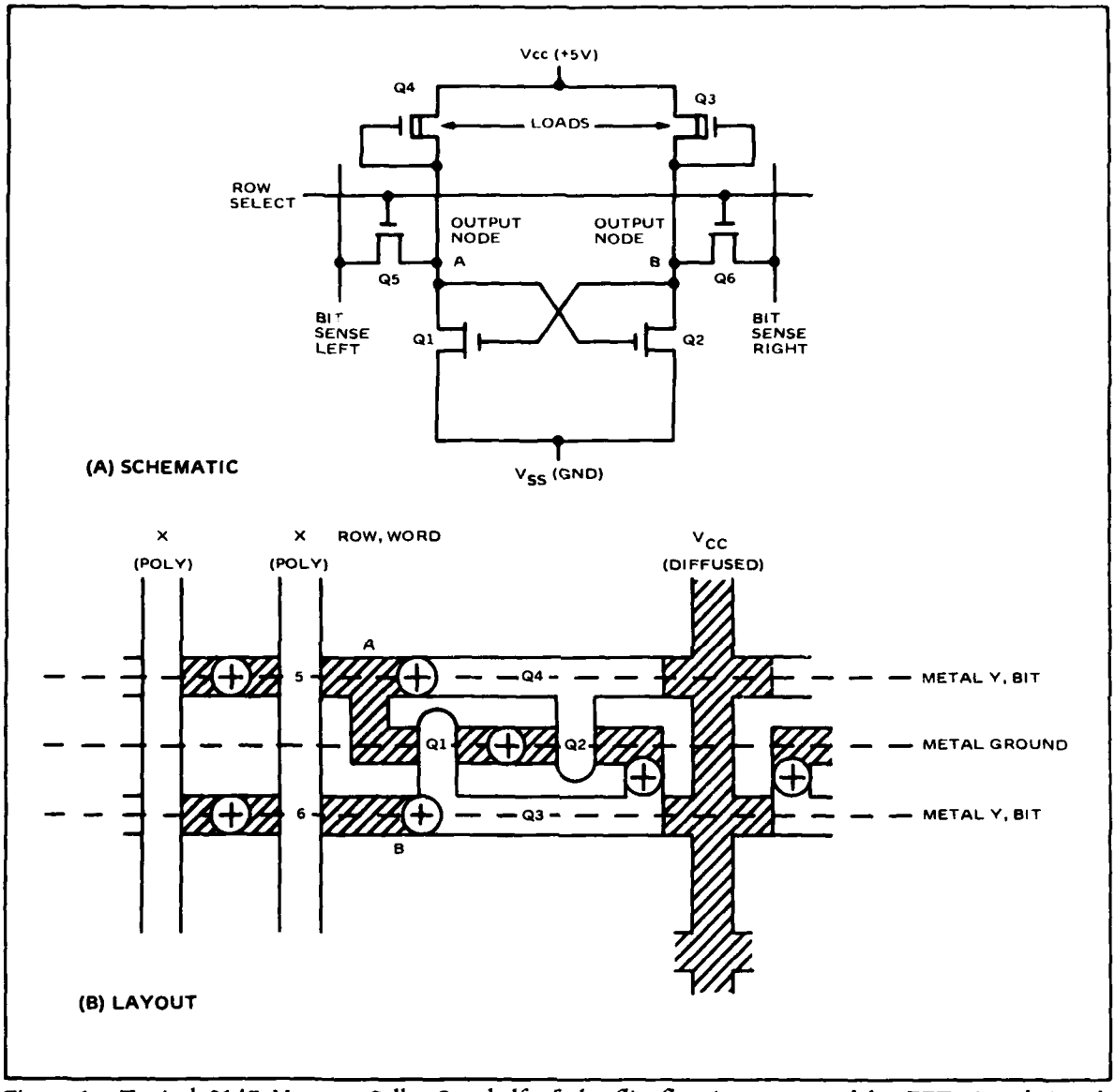


Figure 1. Typical 2147 Memory Cell. One half of the flip flop is represented by FETs 1 and 4 and the other half by FETs 2 and 3. The layout is physically symmetrical to the ground contact between FETs 1 and 2, thus making the physical balance easier to visualize. Equal size of conductors and FETs in length and width leads to equal electrical parameters of conductor resistances and capacitances and transistor gains. Matching of transistor thresholds $V_t$ and leakages is controlled primarily by material processes and only indirectly by physical dimensions.

2. ANALYSIS OF CELL UNBALANCE TEST CONCEPT (Continued)

An electrical analysis of the basic FF cell indicates that the most critical area of the cell is the FF output nodes A and B. A well designed and well balanced FF will hold its state under all environmental conditions and dynamic operations. However, if either node leaks more than the other, instability may occur, or the FF will favor one side much more than the other (See Figure 2). Since these nodes are made up of "N" diffusions, metal and/or polysilicon lines, and transistors, they are subject to leakage defects. If the leakage of the nonconducting node approaches or exceeds the conducting current level of the "on" transistor, the FF will easily go into a "stuck" position and the error will be quickly found by conventional testing. However, if the leakage is less than the conducting transistor current, it may not be found by conventional testing because the FF may still be controllable during normal testing procedures and normal worst-case test conditions. Thus, it appeared that investigations into FF marginal unbalance detection methods to show potential unbalance failures, would prove to be a worthwhile goal.

Further analysis of the memory cell connected to the buffer amplifier (Figure 3) shows that excessive leakage in the I/O line may cause all the flip-flop cells that are connected to that line to fail in a stuck position whenever they are addressed. This would be reflected in a memory status map. During the address selection mode, the FF has the nodes A and B connected to the "N" diffused bit lines and the I/O bus. Even if the FF cell is well balanced, any excessive leakage in the bit lines or I/O bus may unbalance the FF during bit address selection time. If the bit line leakage exceeds the FF conduction current (typically 1 microampere) and the pull-up current from transistors Q1 or Q2, then the FF may reset and stay in a stuck position.

As previously stated, this type of failure can be easily found by conventional test methods. However, nodes A2 and B2 are charged by transistors Q11 and Q12 during the time the chip is deselected. Once the chip is selected, these nodes will leak current away until the Y address connects them to node A1 and B1 respectively. Transistor Q6 or Q7 is expected to hold the charge of A2 or B2. Therefore, a good check of nodes A2 and B2 is to leave the address and chip select signals on long enough to see if transistors Q6 or Q7 can overcome any excessive leakages at these nodes.

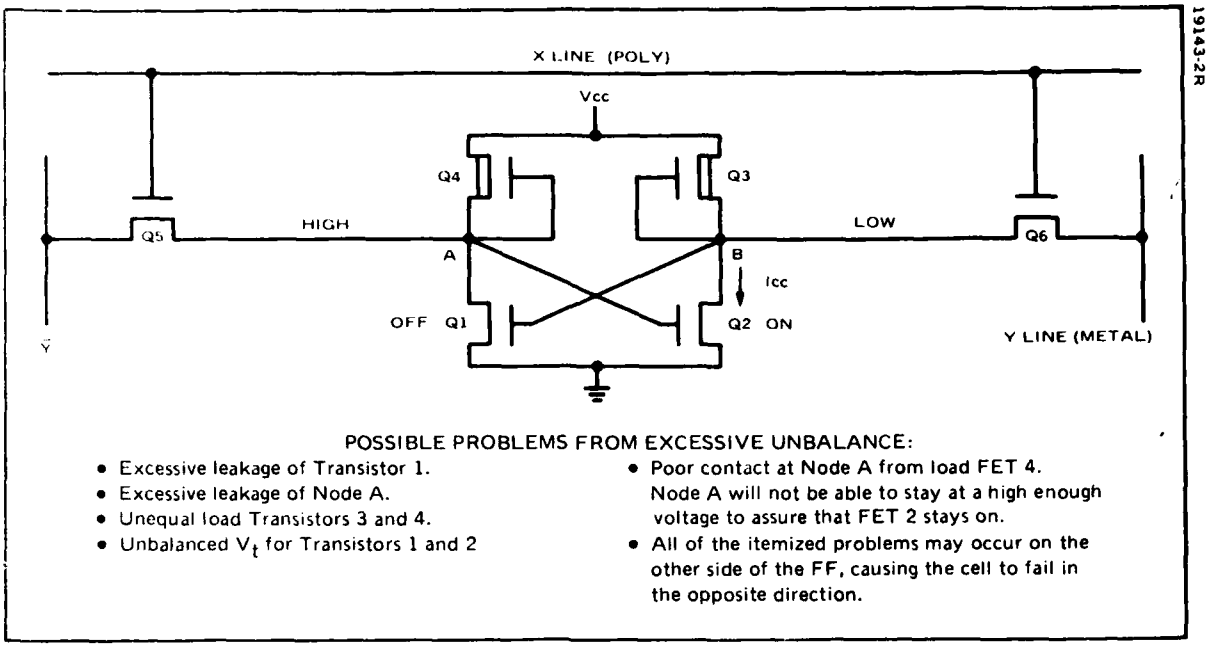


Figure 2. FF Memory Cell Unbalance Factors.

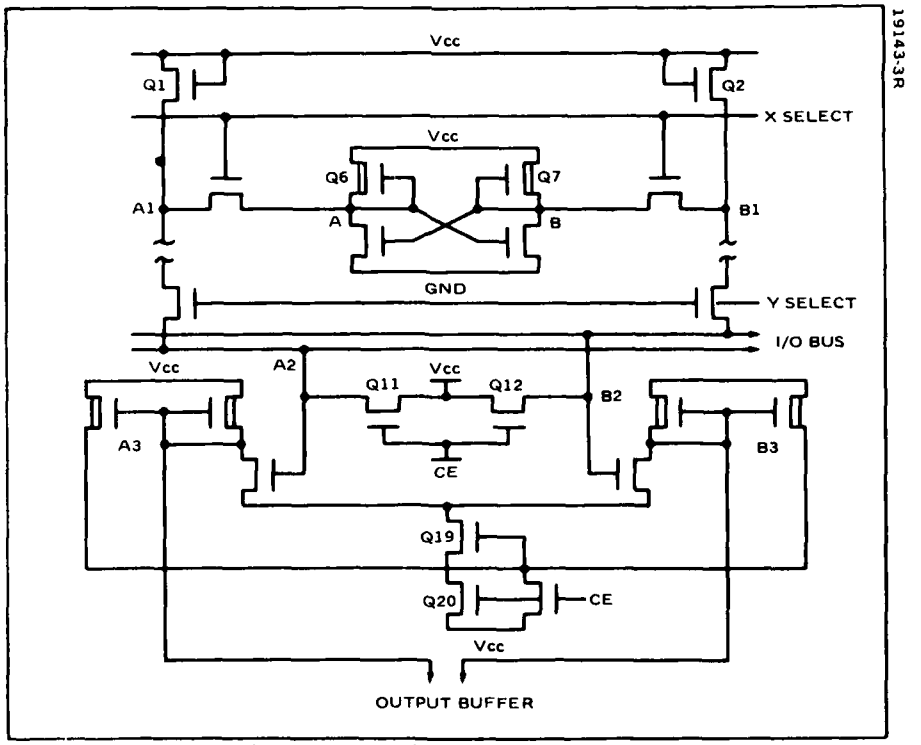


Figure 3. Partial Schematic of the RAM Cell, Column, and Output Sense Amplifier Circuitry. Defects at A1 or B1 or in the I/O bus can upset or modify cell output data.

## 3. DESCRIPTION OF Vmin TEST FOR CELL UNBALANCE

The memory FF cell unbalance can be detected by a prescribed sequence of operations that attains a low critical value of the $V_{cc}$ supply voltage called Vmin, or the cell unbalance value. When Vmin is determined for a memory, a physical matrix display (memory cell map) of the results can be graphically shown as an analysis tool.

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The selected method of determining FF unbalance is to slowly lower the supply voltage while continuously monitoring the FF outputs (Reference 2). As the supply voltage approaches the threshold levels of the active FF transistors, eventually it will reach a point where the conducting transistor can no longer conduct any appreciable current. At this point, the "on" transistors are near the cutoff point, and the leakage balance of Nodes A and B or the $V_t$ balance of the transistors will determine the state of the FF. If the FF is biased in one direction by leakage or transistor threshold unbalance, it may change state prior to complete cutoff of the "on" transistor. Therefore, it is critical that the supply voltage change be made in very small increments when approaching transistor cutoff, so that voltage measurements are accurate. The procedure to check the cell unbalance margin is to decrease the $V_{cc}$ supply in small increments, check the result by returning to the normal voltage level after each decrease and perform an FF cell status check. As shown in Figure 4, the $V_{cc}$ voltage is decreased and then increased by the same amount, after which the cell status is read to see if a cell change has occurred. It was determined that a likely method of detecting and recording unusual FF unbalance is to first put the memory cell in the "unnatural state" and then conduct the Vmin test (as above). The unnatural state is defined as the opposite of the state the FF wants to assume when power is first turned on (natural). All FFs tend to favor either the "1" side or the "0" side. An unnatural state for the memory cells is achieved by writing the opposite to the favored states into the memory. After placing the memory into the unnatural state, $V_{cc}$ is incrementally lowered. It will eventually reach a point where the transistor threshold will be reached and the FF will flip over to its favored, natural state. At this time, if the value of $V_{cc}$ is recorded, a memory cell map of the returned state of each cell in the entire memory can be shown as a function of $V_{cc}$ attained independently for each cell. A computer program has been written to display the Vmin values, in matrix form, as a function of each cell's position in the memory (Reference 3). Such a map is shown in Figure 5.

Most of the cells in the map maintained their unnatural state until $V_{cc}$ was reduced to 0.856 volt, at which time the first group of cells reverted to their natural state. No further reduction in $V_{cc}$ was made, since Vmin for the memory was determined. The topological map of figure 5 is based on a bit map from the suppliers that shows the true physical relationship of the map to the actual device.

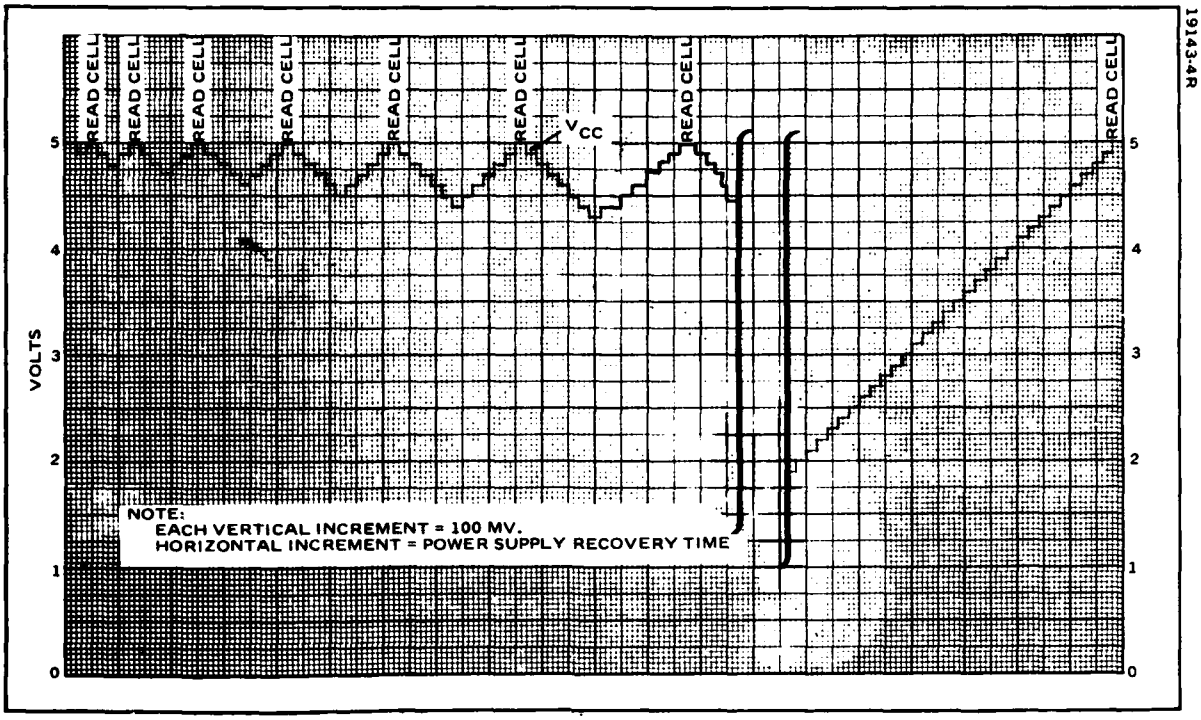



Figure 4. FF Cell U· '·alance Detection. $V_{CC}$ is lowered in small increments and returned to its original level, whereupon the FF cell status is checked to see if it has changed state. The $V_{CC}$ is progressively lowered 100 mV more after each verification. When an FF cell changes state from its original value, the lowest $V_{CC}$ value attained at this time is recorded. All cells in the memory are checked one after the other in sequence.

## 4. DESCRIPTION OF TDF TEST

The time delay failure is a type of malfunction in a static memory, in which a failure is detected a fixed time after a device has previously passed all electrical tests. Generally this type of malfunction is traceable to one or more of the memory FF cells.

The time delay failure (TDF) test consists of first a functional test that examines every cell in the memory by exercising the access time measurement using an all 1s test pattern and a second pass with all 0s. After a part passes this initial room temperature test, then following a time delay of five seconds (subsequently reduced to three seconds) the same functional test is re-run. If a functional failure is detected, a memory cell map is printed to identify the bad cell or cells (see tables 4 and 5). Subsequently a rudimentary failure analysis is performed to determine the exact cause of the cell malfunction. Similar failures of this type have been reported by others (reference 7) showing a poor connection from the FF lead resistor (Polysilicon) to the $V_{CC}$ or the transistor. The FF layout of Figure 1B shows that similar potential problems could occur at the silicon gate contacts of transistors Q3 and Q4 to the N disffusion in three areas: near node A, near node B and between transistors Q2 and Q3.

In essence this type of time delay failure test is dependent upon placing the FF cell into its unnatural static state and allowing the flip flop to fall back into its natural, biased state. The time to fall back into the self-biased state is dependent upon the RC time constant with the C being constant but the R being modified by either a poor contact or excessive node leakage. This time delay is also strongly influenced by temperature, as discussed in section 3.

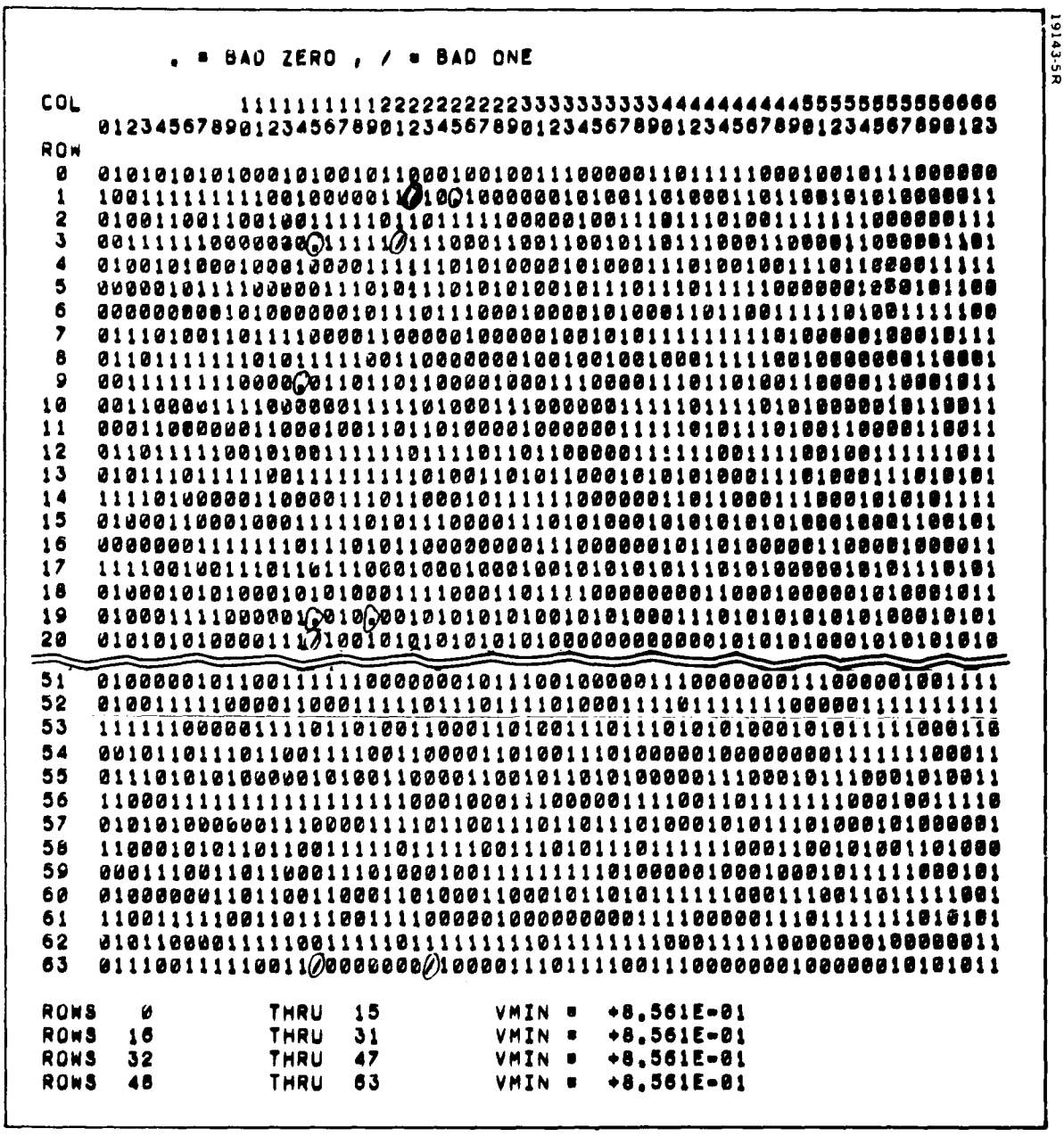



Figure 5. RAM Cell Status Map for Vmin. Each col/row intersection represents an FF memory cell whose state is indicated as (1) or ($\phi$) (state unchanged) or (/) or (•) (state changed). The state changes are located by a visual search. To help identify the changes states they have been encircled.

## 1. ANALYSIS OF DYNAMIC RAM CIRCUIT OPERATION

A review of dynamic RAMs shows that both the memory cells and peripheral circuits use complex clocked circuitry that can create timing problems and related failure modes.

Unlike static RAMs, dynamic RAMs generally do not use any static circuits. This is to save chip space and minimize power consumption. Clocked dynamic circuits are space and power efficient but more complicated than static circuits. Both the memory cells and periphery circuits utilize dynamic circuits. This holds true even for the newer 64K dynamic RAMs. Both the 9050 and the 4050 utilize a single-capacitor memory cell accessed by one MOS FET.

The basic memory cells for the 4050 and the associated sense amplifier are shown in Figure 6. The memory cell uses a polysilicon gate, polysilicon capacitor plate, diffused bit lines, and metal word lines.

A review of various methods of constructing the one-transistor, one-capacitor memory cell shows that the basic principle of charge refresh for the dynamic memory is fundamental to the 4K AMD9050 or TMS4050 type as well as the latest 64K memories (Reference 4). The memory cell still depends upon the basic parallel capacitance of a back biased P-N diode and a silicon dioxide dielectric capacitor. The basic memory cell layout is shown in Figures 7 and 8. The P-N junction diode is the dominant capacitor that loses charge rapidly with time and high temperature (Reference 5).

In Figure 7A the schematic shows one FET connected to two capacitors in parallel. One capacitor is a normal parallel plate device with a silicon dioxide dielectric. One plate is formed by the polysilicon and the other plate when the inversion layer is created. The other, more dominant, capacitor is a PN junction diode that is created when the polysilicon plate is charged to $V_{dd}$ and the inversion is formed. Access to the capacitors is made when the word line turns FET (Q6) on and connects the capacitors to the bit line. Figure 7B shows a cross section of the memory cell showing how the capacitors physically connect to the bit line.

Circuit innovations and improvements in process technology have reduced refresh time requirements, but the memory capacitors still leak charge and are still subject to processing defects that cause excessive charge leakage. Figure 9 shows the typical refresh time required versus temperature, and the maximum refresh time specification limits at various temperatures. It should be noted that a considerable gap exists between the typical refresh time expected and the specification limit. This gap is necessary because the leakage rate of the memory cell capacitors is highly temperature dependent and the actual leakage rate is not precisely predictable. In order to reach the higher temperatures for military applications, the refresh times had to be reduced to 1 millisecond for 85°C and 0.5 millisecond for 100°C (MIL-M-38510/235A).

The 9050 and 4050 N channel memory devices are packaged in an 18-pin DIP. A MIL-M-38510/235A specification has been written on this device. All input signals are fully TTL-compatible except the single high level clock signal called Chip Enable (CE). When the CE goes low, the memory is internally precharged and assumes its low power standby mode. All operating cycles are initiated when the CE goes high. Read out is nondestructive so that rewriting is not necessary. Successive read and write operations at the same location can improve performance, since readdressing is not required. This combination is specified as a Read/Modify-Write cycle.

Data In and Data Out signals are bused together on a common I/O signal line. An external pull-up resistor is used for TTL compatibility. Input and output data are the same polarity.

Refresh of the cell matrix is done by performing a memory cycle at each of the 64-row addresses (A0 through A5) every 2 ms at 70°C, 1 ms at 85°C, or 0.5 ms at 100°C.

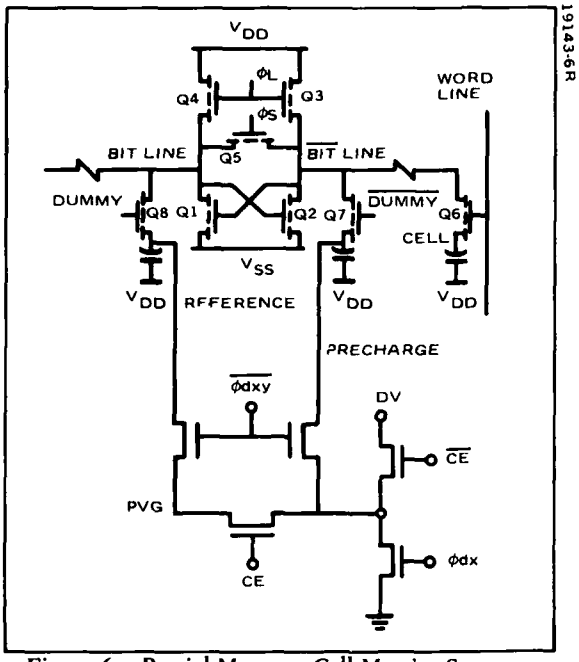



Figure 6. Partial Memory Cell Matrix, Sense Amplifier, and Precharge Voltage Generator for the 4050 RAM. Dynamic clocked circuitry is used extensively in the sense amplifier and precharge voltage generator.

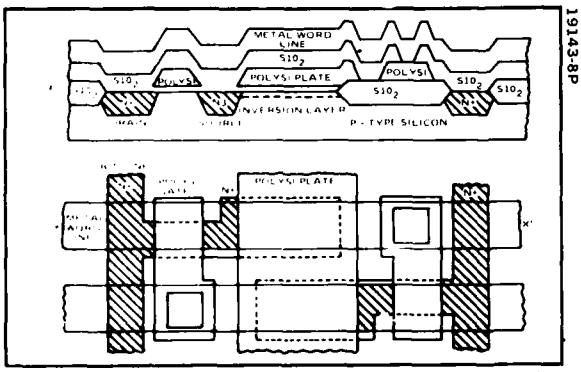



Figure 8. Typical 4096-Bit Dynamic RAM Cell Layout and Cross Section. Single polysilicon cell with diffused bit line. The cross section shown in (a) is taken along the line XX' in (b).

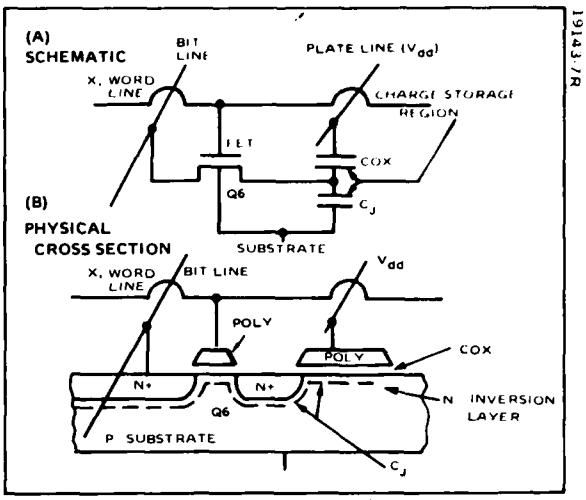



Figure 7. Dynamic RAM Cell Structure. The memory cell capacitor is dependent upon $V_{CC}$ to create the N inversion layer as one of the capacitor plates.

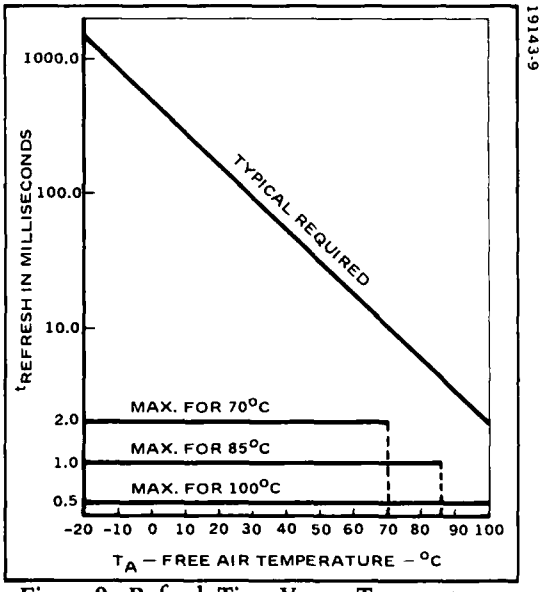



Figure 9. Refresh Time Versus Temperature. Room temperature tests at 2 ms leave too large a gap for screening out marginal devices.

## 2. DESCRIPTION OF DYNAMIC RAM TESTS

**Three electrical test parameters were selected to provide three different test approaches. Refresh time is directly relatable to back-biased diode leakage, the chip enable pulse allows measurement of dynamic circuit drive capability, and V-BUMP allows measurement of the sense amplifiers read level margin between "0" and "1".**

Extensive investigations have shown that results of DC and AC parameter tests of dynamic RAMS are generally quite predictable. However, major differences can occur in functional pattern testing from one dynamic memory to another, depending mainly on whose original design was utilized. Even the so-called second source supplier may require an entirely different set of functional test patterns if identical mask sets are not used. The main problem with test patterns is that they can become too long.

Effective function tests for memories are highly dependent on the memory chip architecture, topological layout, sense amplifier, cell design, internal timing generators, and often the type of internal peripheral circuits being used. Even if the same device processes are used, the test patterns would still be different due to the different chip architectures and device structures from various manufacturers. Therefore, test patterns are deterministic and long test patterns need not be applied indiscriminately. Fortunately, both the 4050 and 9050 have similar memory layout patterns, using single-layer polysilicon.

Often test patterns developed for a primary supplier will not effectively test alternate source devices. The alternate supplier should be questioned to determine what test patterns are necessary for his parts. Regardless of any supplier's advice, the user must decide on an adequate test plan for qualifying the device, and screening the device upon its receipt from the manufacturer.

Investigation of numerous electrical test parameters as candidates for dynamic RAM testing resulted in the selection of the following: memory cell refresh time $T_{RF}$, chip enable pulse $T_{WCEH}$ and $T_{WCEL}$, and memory cell charge margin V-BUMP.

Memory Cell Refresh ($T_{RF}$) Test – Normally, refresh time is specified as the maximum time limit allowed before a cell must be recharged to a full "1", or else the cell may lose its charge status. Thus, each cell has a storage time associated with it. The storage time of any dynamic MOS RAM can be expressed by the empirical equation:

$$t_{STORAGE} = A \exp(-BT),$$

where T is junction temperature in °C,
B is a variable relating the magnitude of the generation-recombination current to the junction temperature (units of 1/°C), and
A is a scaling constant reflecting such variables as junction area, bulk defect density, and sense amplifier design.

Note that the term "B" in the equation is not a constant. Conventionally, it is assumed that the storage time doubles for every 10°C decrease in junction temperature, which is equivalent to assuming that "B" is 0.055, but it does in fact vary at least 30% from this typical value.

Since the refresh test is a fundamental test that applies to all dynamic memories, this test was initially studied extensively. To be *effective, this test must be used on all dynamic memories at the highest* operating temperature. The capacitance leakage factor for the diode portion of the capacitor is bulk saturation current dependent, and therefore is difficult to guard band efficiently at room temperature.

Chip Enable Pulse (TWCE) Test - Another test considered is the "long cycle time", in which the opposite end of the speed spectrum is investigated. All functional tests are based on maximum speeds and short cycle times to keep test times short and efficient. The effect of short off periods (precharge time) may reveal some hidden problems of circuit design weaknesses, or excessive leakage at the precharge node. In addition, sustaining a long active drive cycle (low frequency operation) may reveal peripheral amplifier problems.

Excessive leakage may also occur in the active stage of many of the internal timing generators that depend upon MOS bootstrap circuits. All of the new 64K dynamic RAMs with the 5V supply depend heavily on this type of circuit to boost the voltage levels of critical nodes. Normally all internal signals have at least one threshold drop when signals pass through gates and amplifiers ($V_{dd}$-$V_t$). In order to boost the signal levels back up to at least $V_{dd}$, typical bootstrap circuits as shown in Figure 10 are used. Node X generally gets boosted to 1.5 to 2 times $V_{dd}$ through *feedback capacitor C, so that the output voltage Vout does not see the* $V_t$ drop. However, Node X cannot hold its charge indefinitely and must be recharged periodically. Y is a normal input of the amplifier, while $\phi$ for circuit (B) is a $V_{dd}$ level clock.

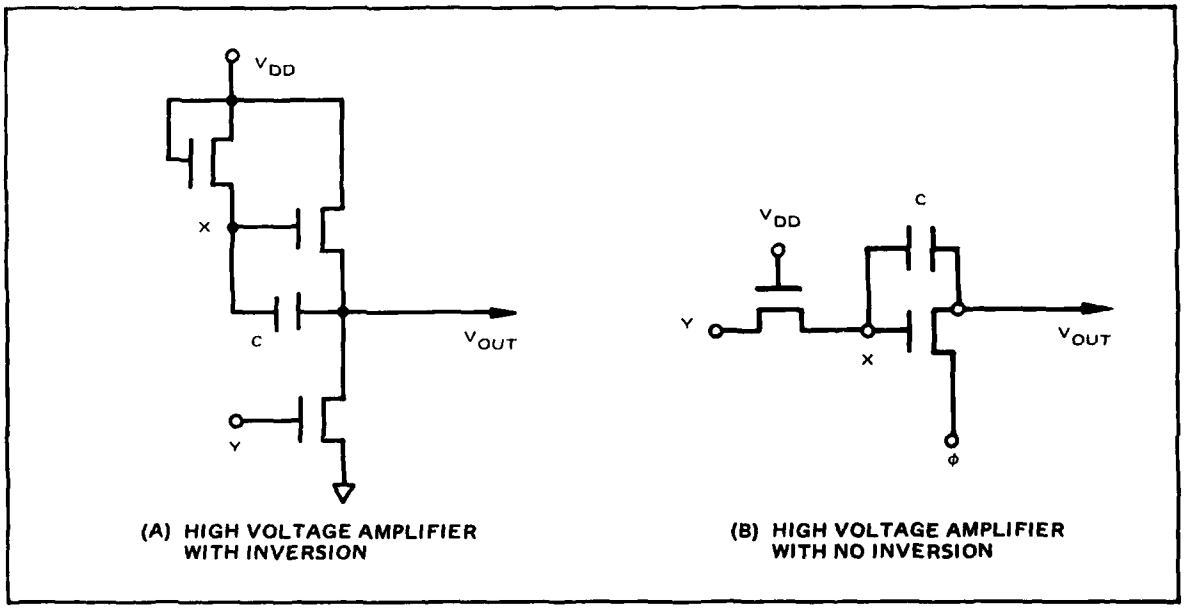



Figure 10. MOS Dynamic Bootstrap Amplifiers. These typical circuits are used to boost the signal levels back up to at least $V_{dd}$.

2. DESCRIPTION OF DYNAMIC RAM TESTS (Continued)

The chip enable (CE) signal is basically a clock. When it is high ($T_{WCEH}$), the sense amplifiers are activated, internal memory cells are selected, and data is written or read out. When the CE pulse is low ($T_{WCEL}$), then most internal dynamics circuits are precharged. However, there are some circuits that are actually activated during this low period. Therefore, the CE pulse width effects must be evaluated at both levels.

V-BUMP Test – A test for weak margins in sense amplifiers used to detect faulty "1" and "0" is the so-called V-BUMP test that can be used when both $V_{dd}$ and $V_{bb}$ are available in the memory device. The new 64K dynamic RAMs have gone to a single supply voltage scheme which reduces the effectiveness of the V-BUMP test, since $V_{bb}$ control of transistor threshold is lost. One memory cell concept has the polysilicon plate grounded rather than connecting to $V_{dd}$, which eliminates all use of the V-BUMP test.

All sense amplifiers have a margin between the "1" level and the "0" level when reading a charge in the memory cell. Both memories, the 9050 and 4050, use the $V_{dd}$ supply for one side of the capacitor plate in the memory cell as shown in Figures 7 and 8 of the previous topic. In addition, the substrate is biased with the $V_{bb}$ supply. The voltage bias on the substrate affects the FET threshold: the more negative it becomes, the higher the transistor $V_t$ will go (Reference 6).

The V-BUMP process starts by writing "0" in all the memory cells. With $V_{dd}$ low and $V_{bb}$ at maximum, a minimum charge is placed in all cell capacitors. Then the voltages are bumped up to the opposite extreme values making the sense amplifiers more sensitive, and the memory cell capacitors decrease in capacitance value slightly. The diffused diode portion of capacitance will decrease as the $V_{dd}$ voltage increases, the voltage in the capacitor will rise since the charge remains constant. In essence "0" status charge in memory cells will increase slightly in voltage and the sense amplifiers will be slightly more sensitive, and may see high "0" as a "1". Any cell that reads a "1" instead of "0" is regarded as a failure.

Conversely the condition for a "1" is normally checked for worst case conditions during functional tests and AC parameter tests. However, worst-case voltage conditions were added to write and read all "1s", and called V-BUMP(1).

## SECTION 3
## DEVICE SCREENING FOR SUSPECT PARTS

## 1. SCREENING OF STATIC RAMs FOR CELL UNBALANCE AND TDF

In order to verify the validity of the two selected test parameters, they were used in two screening tests to identify suspect parts for verification of failure in later life tests. The number of suspect parts found was adequate for the cell unbalance test methods (18 out of 5000), but inadequate for the TDF method (2 out of 5000).

During receiving inspection, static RAMs are subjected to standard tests at room temperatures only, and are expected to have reject rates much less than 0.5%. The receiving test philosophy at Hughes is to run the high speed functional tests first because they provide the fastest go/no-go testing over the entire chip. No further testing is necessary if a device fails any functional test, because it is then rejected. Test patterns are selected based on experience and vendor recommendations. If the parts pass functional tests, then DC and AC parameters are tested in that order.

The two new tests that were selected (cell unbalance and TDF) were implemented to determine their relative effectiveness in screening for faults on parts that pass normal go/no-go testing. The first test was the low Vcc voltage test to check for excessive node unbalances in the FF memory cells. The second test was the time-dependent failure (TDF) screen that identifies initially good devices that fail later as a function of time.

Cell Unbalance Test Results – The cell unbalance test required initial characterization of static RAMs to determine the low Vcc setting needed for a fast and practical inspection screen. Twenty-five Intel 2147s from one lot and 20 Intersil parts from four lots were characterized. The Intel parts would hold their cell status down to a $V_{cc}$ minimum of 1 volt and the Intersil parts to 0.9 volts. Reviewing the lot-to-lot distribution for Intersil parts, a $V_{cc}$ minimum voltage of 1.4 volts was selected for the initial screen of recently purchased Intersil static RAMs. Any part that could not hold its "1" or "0" state to a $V_{cc}$ minimum of 1.4 volts was rejected and held for further investigative evaluation.

Over 7000 Intersil 2147s were tested at receiving inspection, and a total of 18 parts were obtained that exceeded the minimum $V_{cc}$ of 1.4 volts. These parts were then pulled from the line and fully electrically characterized. The testing included the two special tests, at three temperatures: 25°C, -55°C and +125°C. This data was necessary to compare after life tests were run.

TDF Past History – For the TDF screen tests, reviewing past investigations by others on time-dependent failures (Reference 7), unit periods up to 10 seconds had been used by Eugene Hnatek, et al. Hnatek reported that two failures out of 50 parts (4K static RAMs) were detected at 25°C in a 3-second period. These parts passed all normal functional, AC, or DC tests as long as the cell was addressed at least once every 3 seconds.

Failure analysis disclosed that these parts had a defect in the static memory cell in which one of the 60-megohm polysilicon pull-up resistors had an open contact. This means that whenever a "1" was written into the node that had a high resistance contact from resistor to $V_{dd}$, that node would not change to a full "1" or be able to sustain a "1". Then the FF would flip over and stay in the opposite state. As in a dynamic RAM cell, the error in this static FF cell might not be found during normal fast pattern testing.

In both the Intel and Intersil 2147 static memory cell, the pull-up is by a depletion-mode MOS FET. Poor contact between the diffused drain or source to the polysilicon could occur, but it is highly process and mask technique dependent. There are six contacts shown, in Figure 1B, but two of the contacts to the metal Y lines are shared with the next cell. There is metal ground contact between FETS Q1 and Q2. The other three contacts are polysilicon to the N+ diffusion. Under-etching within the via holes for any of these contacts can cause poor contact problems.

TDF Test Results - Initial screening, using the two special test techniques on approximately 5,000 Intersil 7147 devices identified 18 potential probem devices using the low Vmin method, and 2 actual failures using the TDF method. Normal DC, AC, and functional tests on these candidate devices, were performed at -55°C, +25°C and +125°C to determine if any unusual characteristics could be immediately revealed.

It was determined that due to tester limitations, it was much faster to use the all "1" and all "0" test patterns in two separate operations to find the "flip-over" characteristics as a function of decreasing $V_{CC}$, rather than using the unnatural state. The concept of placing the static cell into its unnatural state was good, but the Sentry 610 has limited core capacity and this test consumed too much tester memory and would have had to be off-loaded onto a disc. Obviously the manual disc operation would take too long and was discarded for the all "1" and all "0" test pattern technique. A checkerboard and complement checkerboard test pattern would have worked just as well but the visual display would not allow easy discernment of "flip-over" states.

The two devices that failed the initial TDF screen were "good" devices that passed all normal functional, DC, and AC tests. However, when a time delay of 5 seconds was used and the functional test performed again, the devices showed a definite failure indication. A recently developed memory cell map technique was utilized (Table 4) which shows that the cell at coordinate Row 0 and Column 29 failed on device No. 274. Table 5 shows that device No. 282 failed in two cells at Row 11, Columns 11 and 12. Both parts failed when an all "0" pattern was written, and the particular cells changed state to a "1" at a $V_{CC}$ of 5 volts. These are the results of testing at room temperature using nominal voltage, timing, and speed.

The initial characterization test results on the two TDF parts are shown in a matrix format (see Table 6) to allow easier analysis. The initial analysis does indicate some interesting results. For example, both device failures are temperature dependent. Device No. 274 failed at 25°C and +125°C, but passed at -55°C even after the 5-second delay. Device No. 282 failed normal tests at high and low temperatures before the TDF screen. After the 5-second wait period, the device failed even at room temperature, which makes this TDF test an encouraging screening tool if high temperature tests are not practical for certain types of inspections.

Further electrical tests of device No. 274 showed that its weakness could be detected by using the Vmin unbalance test with high temperatures (see Figure 11). Since both TDF devices were temperature sensitive, these types of failures could be found using a fast Vmin test but with the inconvenience of having to use high temperatures.

1. SCREENING OF STATIC RAMs FOR CELL UNBALANCE AND TDF (Continued)

TABLE 4. MEMORY CELL FAILURE MAP - 7147 NO. 274

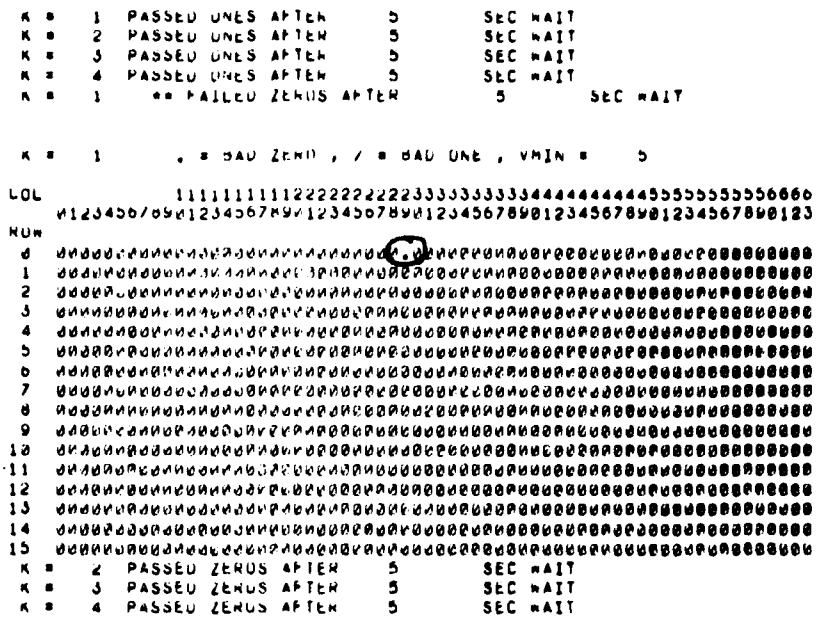
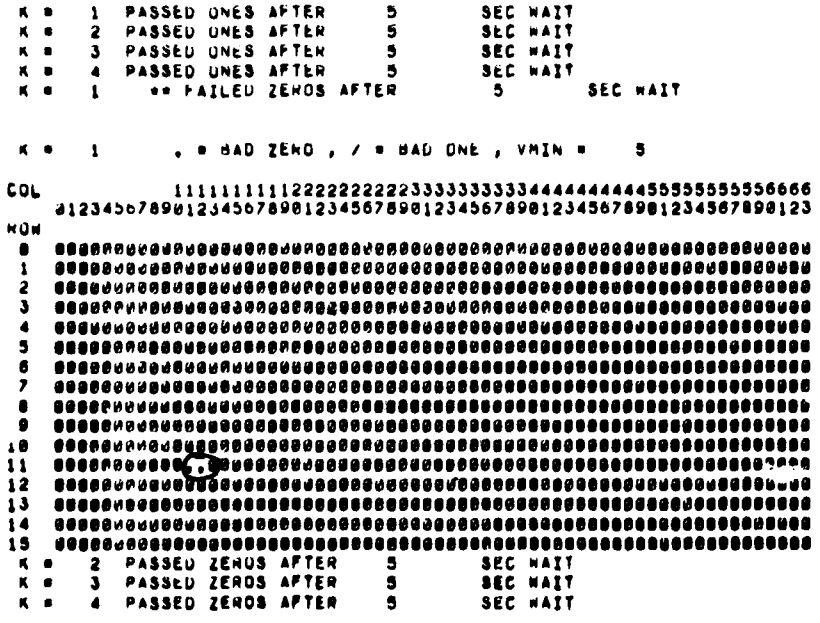



TABLE 5. MEMORY CELL FAILURE MAP - 7147 NO. 282




Encircled cells in Tables 4 and 5 indicate the TDF cells.

TABLE 6. 7147 STATIC RAM TEST RESULT MATRIX

| Device No. 274 | -55°C | +25°C | +125°C |
|---|---|---|---|
| Functional | P | P | P |
| DC | P | P | P |
| AC | P | P | P |
| TDF 5-sec Functional | P | F | F |
| $V_{0l}$ (1) | F(>2V) (2) | P | P |
| $V_{0h}$ (1) | F(-0.7V) | P | P |
| $V_{min}$ | P(0.8V) | P(0.8V) | F(>2V) (2) |
| **Device No. 282** | **-55°C** | **+25°C** | **+125°C** |
| Functional | F | P | P |
| TDF5-sec | F | F | F |
| DC | P | P | P |
| AC($t_{AA}$, $t_{CS}$) | F | F | F |
| Vmin | F(>2V) (2) | F(>2V) (2) | F(>2V) (2) |

(1) Fixed at address "0" only.
(2) Further quantizing tests are required to determine exact Vmin voltage for each chip at that temperature.
(3) P = Passed
F = Failed

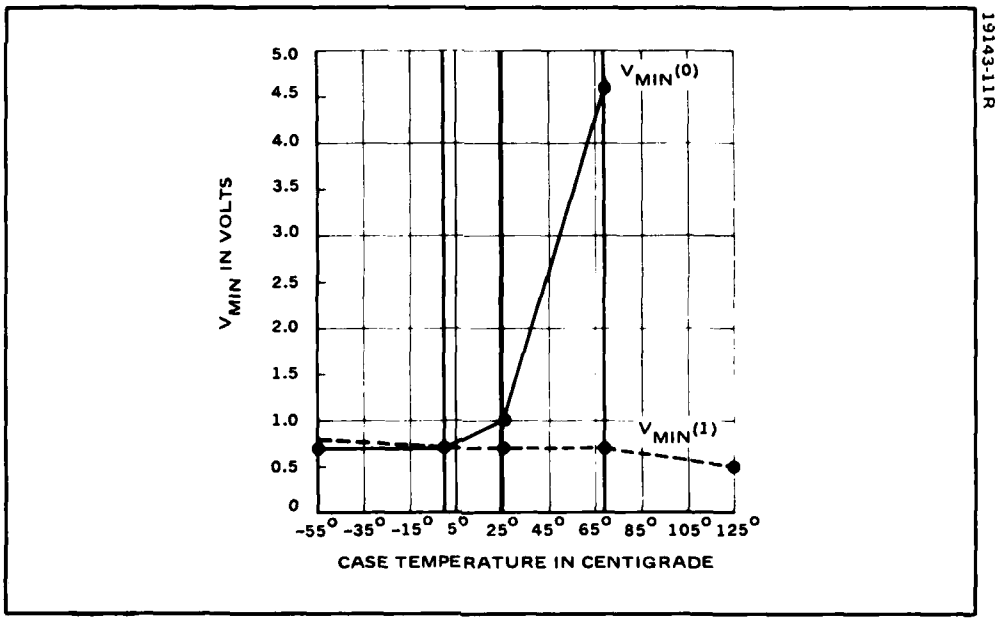



**Figure 11. $V_{min}$ Characteristics of Device No. 274. The $V_{min}$ test at elevated temperatures can easily detect this type of TDF.**

## 2. SCREENING OF DYNAMIC RAMs

Three special test parameters, (1) refresh time (TREF), (2) chip enable pulse test (TWCE), and (3) sense amplifier margin test (V-BUMP) were selected and used for initial screening of over 5000 dynamic RAMs. Only 18 devices were found that could be utilized in the accelerated life tests.

Refresh Time (TREF) - Since only room temperature tests were being utilized, the refresh time requirement was increased from 2 milliseconds to 10 milliseconds to screen most of the dynamic RAMs, but no rejects were found. The primary method of screening depended extensively on refresh time measurements because of its known operational limitation that depends upon well-defined physical leakage parameters, such as reversed bias junction current. The phenomenon of capacitor cell leakage has been well defined in section 2 as well as the requirement to recharge the memory cell capacitors periodically.

The standard method of refreshing the total memory is by reading one cell out of each row once during each refresh cycle. This permits the fastest refresh possible by addressing all 64 rows and not changing any of the column address lines. The 9050 and 4050 memory devices refresh the entire row if any bit in a row is address. The Sentry hardware pattern generator uses this standard method of refreshing the memory. In order to do an effective refresh test, the standard refresh test program was modified to allow each individual cell to be measured separately and to read all bits in the rows first, rather than reading all the bits in the columns. When the first row is completed, the next row is activated and measured, one cell at a time. This is repeated until all 64 rows are checked. This means that at the end of the last bit, approximately 2 milliseconds have elapsed if the bit cycle time is 490 nanoseconds. Longer times can be measured with coarser resolution, depending upon the requirements.

It was planned to characterize the refresh time distributions among the 4096 memory cells of each chip using the memory cell map technique. It is known that refresh times tend to have a normal distribution within a memory, with a few cells showing low refresh times as deviants (Reference 5). Figure 12 shows a typical refresh cell map for the dynamic RAMs (9050 and 4050). This particular refresh cell map measures individual cell refresh measurement times, or the actual minimum storage time required of each individual cell. The two worst case cells Ø and 1 have been encircled at row 16, column 59 and row 0, column 33. Cell Ø fails refresh time between 2.0 and 4.8 milliseconds. Cell 1 fails refresh between 4.8 and 7.6 milliseconds. The refresh cell map has been topologically arranged utilizing the vendor bit map data.

The coded symbols distributed randomly over the map show the relative range of refresh time for each cell failure. The blank spaces on the refresh bit map indicate that refresh time exceeds 0.3 second. The cell maps on all suspect devices were reviewed for identification of any process related or design-dependent pattern that might provide a clue to potential failures or reliability problems.

CHIP Enable Pulse (TWCE) - The TWCE test was not used for actual screening of the 5000 parts since the test concept was not developed and ready at the time. However, initial tests of TWCEH using the maximum pulse width of 4 us and a TWCEL of 160 ns produced 11 rejects out of the 30 parts selected to be used for life tests. Most of the rejects occured at 85°C.

V-BUMP - The V-BUMP test was utilized at room temperature on 4000 AMD parts that Hughes purchased prior to the time the life test was started;

none failed. When V-BUMP tests were used on the 30 parts selected for life test, 3 of the TI parts were rejected at room temperature, but at 85°C all TI parts were rejected. Therefore, it would have been extremely valuable to have screened the AMD parts at 85°C.

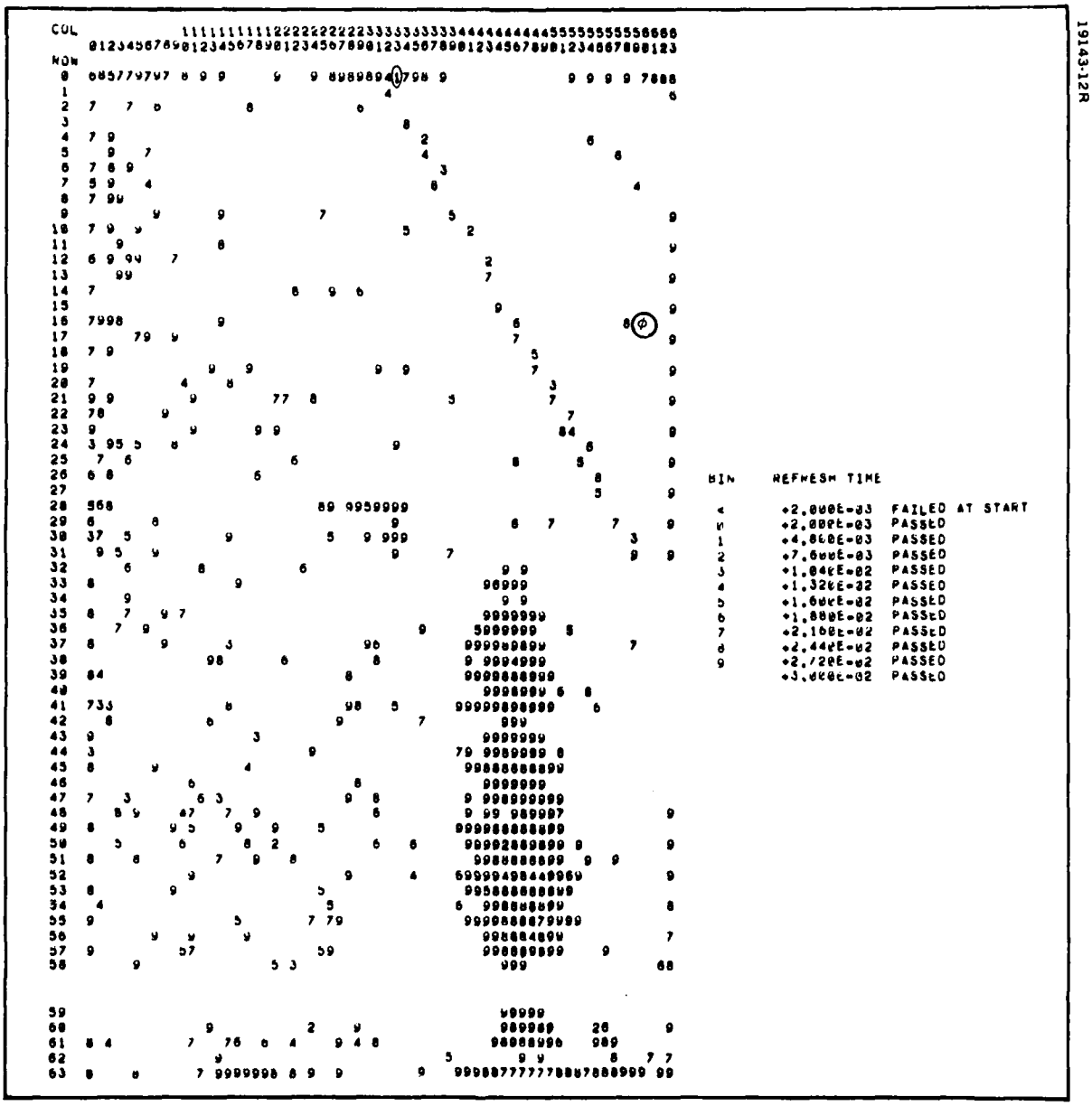



Figure 12. Refresh Cell Map. TA = 85°C. The randomly distributed numbers indicate the relative range of refresh time for each cell that did not exceed the 30 milli-second maximum. The refresh time/bin number table relates the numeric symbols and refresh time. Blank spaces indicate that refresh time exceeded 30 milli-seconds.

## SECTION 4
## EVALUATION OF TEST PARAMETERS

Section 4 – Evaluation of Test Parameters

## 1. LIFE TESTING OF STATIC RAMs

Due to the limited number of suspect parts for use in the life test, a high temperature accelerated life test was conducted. Analysis of the life test data did not disclose any significant failures or trends correlatable with the selected test parameters of the static RAMs.

Screening of parts for both the static and dynamic RAMs did not reveal any large quantity of devices suspected of being potential failures because of their special electrical test parameter values. Over 12,000 parts were screened and only 18 suspect devices from each part type were found. Consequently, plans to life test 102 devices of each of the two memory types at 125°C were found to be infeasible.

Insufficient suspect devices were found even though over 7,000 devices were screened using the identified selection criteria for static RAMs. Over 5,000 parts were screened for the dynamic RAMs, with similar results. Such a limited number of samples demanded that elevated temperature testing be conducted in excess of the planned +125°C, in order to achieve a significant number of device hours of life testing. The original plan called for testing 102 devices for 1000 hours at 125°C, while the new plan tested 30 parts for 500 hours at 200°C. Although the new test plan called for a life test duration of 500 hours, it was determined that continuing the life test to 1000 hours would require only a small amount of additional effort. Therefore the test was continued for another 500 hours and extra data was gathered.

A temperature step stress plan was formulated to find the highest temperature at which a device can operate for the life test, and to provide a preliminary look at the suspected device parameter for failure trends. (See Appendix A for details of the temperature step stress plan.)

Life testing of static RAMs resulted in a number of functional failures but no discernible trends towards failure for the selected electrical test parameters. The results of life testing detailed in Appendix B are summarized in Table 7. A total of nine functional failures occurred and they were all attributed to open $V_{CC}$ lines caused by metal electromigration. Any voltage reading equal to 5 volts is a failure. Analysis of the data showed no evidence that metal electromigration failures are related to the excess FF cell unbalance conditions.

Inspection of the data in the table showed no discernible drift characteristics of the devices at +125°C. Therefore, statistical data analysis using the Sentry 610 ATE computer was performed. Average values of the selected test parameters from the computer analysis have been plotted in Figures 13 through 18. The plotted average values confirm that the selected test parameters show no significant trends towards failure.

Figure 13 shows a plot of the average value of $Vmin^{(1)}$, for suspect devices, as a function of life test hours at 25°C, -55°C, and +125°C. None of the values have drifted towards higher voltage values, which would mean a drift towards failure. Figure 14 shows the same type of plots for non-suspect devices with the same stable results. Figure 15, for suspect devices, and Figure 16, for non-suspect devices, show plots of Vmin(0) versus life test hours. Again the results show good stability and no drift trends.

Figures 17 and 18 show plots of the difference between Vmin(1) and Vmin(0) versus life test hours for suspect and non-suspect devices. The important criterion here is that the differential voltage does not increase with life. Neither group shows any tendency to expand in differential voltage as a function of life test hours. The conclusion is that these static

TABLE 7. Vmin ELECTRICAL TEST DATA (125°C) FOR 2147 STATIC RAMs SAMPLED DURING 200°C LIFE TEST

| Suspect Devices | Zero Hours | | 500 Hours | | 1,000 Hours | | |
|---|---|---|---|---|---|---|---|
| Ser No. | $V_{min}^{(1)}$ | $V_{min}^{(0)}$ | $V_{min}^{(1)}$ | $V_{min}^{(0)}$ | $V_{min}^{(1)}$ | $V_{min}^{(0)}$ | |
| 101 | 0.7 | 0.7 | 0.2 | 0.7 | 0.7 | 0.7 | |
| 104 | 0.7 | 0.7 | 0.7 | 0.7 | 0.7 | 0.7 | |
| 111 | 0.7 | 0.7 | 0.7 | 0.7 | 0.7 | 0.7 | |
| 113 | 0.6 | 0.8 | 0.6 | 0.8 | 0.6 | 0.8 | |
| 120 | 0.7 | 0.8 | 0.8 | 0.8 | 0.8 | 0.8 | |
| 213 | 1.1 | 3.3 | 1.1 | 3.1 | 5.0* | 5.0* | Failed |
| 252 | 0.7 | 1.1 | 0.7 | 1.1 | 0.7 | 1.0 | |
| 254 | 0.8 | 0.9 | 0.8 | 0.9 | 5.0* | 5.0* | Failed |
| 255 | 0.8 | 0.9 | 0.8 | 0.9 | 5.0* | 5.0* | Failed |
| 263 | 0.7 | 1.0 | 0.7 | 1.0 | 0.7 | 1.0 | |
| 264 | 1.0 | 0.9 | 1.0 | 0.9 | 1.0 | 0.9 | |
| 265 | 0.7 | 1.0 | 0.7 | 1.0 | 0.7 | 1.0 | |
| 266 | 1.5 | 1.5 | 5.0* | 5.0* | 5.0* | 5.0* | Failed |
| 267 | 1.0 | 0.7 | 1.0 | 0.7 | 5.0 | 0.7 | |
| 271 | 1.3 | 1.5 | 5.0* | 5.0* | 5.0* | 5.0* | Failed |
| Non-Suspect Devices | | | | | | | |
| 106 | 0.7 | 0.7 | 0.7 | 0.7 | 0.7 | 0.7 | |
| 107 | 0.7 | 0.7 | 0.7 | 0.7 | 0.7 | 0.7 | |
| 108 | 0.7 | 0.7 | 0.7 | 0.7 | 0.7 | 0.7 | |
| 109 | 0.7 | 0.7 | 0.7 | 0.7 | 0.7 | 0.7 | |
| 115 | 0.8 | 0.7 | 0.8 | 0.8 | 0.8 | 0.7 | |
| 116 | 0.7 | 0.7 | 0.8 | 0.8 | 0.7 | 0.7 | |
| 118 | 0.7 | 0.7 | 0.8 | 0.8 | 0.7 | 0.7 | |
| 119 | 0.7 | 0.7 | 0.8 | 0.8 | 0.8 | 0.7 | |
| 131 | 0.6 | 0.7 | 0.6 | 0.7 | 0.6 | 0.7 | |
| 132 | 0.7 | 0.6 | 5.0* | 5.0* | 5.0* | 5.0* | Failed |
| 137 | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | |
| 138 | 0.5 | 0.5 | 0.5 | 0.5 | 5.0* | 5.0* | Failed |
| 139 | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | |
| 262 | 0.9 | 0.9 | 0.9 | 1.0 | 5.0* | 5.0* | Failed |
| 272 | 1.0 | 1.0 | 0.9 | 1.0 | 5.0* | 5.0* | Failed |

*A 5.0 volt reading means that the device has failed.

RAMs with 77 cells having unbalanced voltages out of the normal distribution are stable and do not pose potential failure problems.

Other conventional, but key test parameters were analyzed to determine if any unusual performance was occurring. Figures 19 and 20 show the average supply current, as a function of life test hours for suspect and non-suspect devices respectively. The suspect devices show a small increase of 5% in average current, while the non-suspect devices show a slight decrease in current of 3.5% at the end of life. The total change of current at the end of life is insignificant and is not related to the special test parameters of interest.

Figures 21 and 22 for suspect and non-suspect devices show plots of average standby current $I_{SB}$ as a function of life test. The plots show that these parameters are stable for both groups of devices.

1. LIFE TESTING OF STATIC RAMs (Continued)

Figures 23 and 24 for suspect and non-suspect devices show plots of average address access times $T_{AA}$ as a function of life. These plots show that both groups of devices have similar characteristics with a slight increase in access of about 4% at the end of life. Again, these results do not relate to the special test parameters of interest.

It was concluded that these electrical parameters are stable.

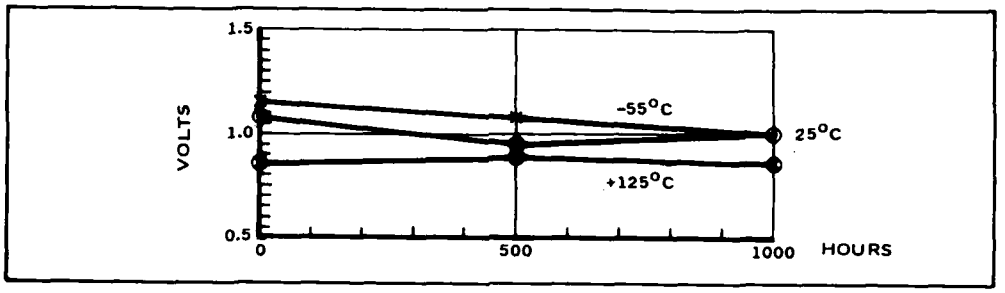



Figure 13. $V_{min}$ (1) for 2147 Suspect Devices

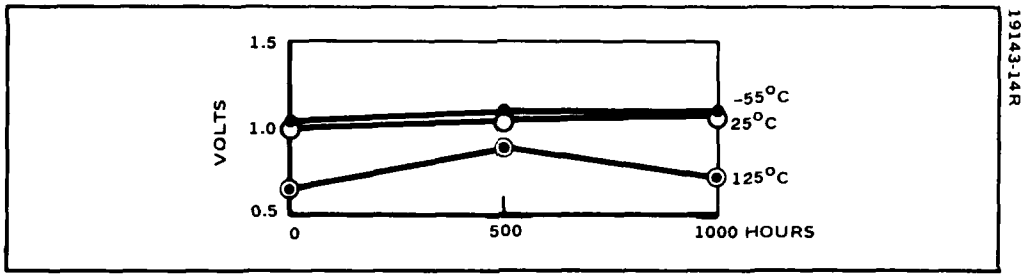



Figure 14. $V_{min}$ (1) for 2147 Non-Suspect Devices

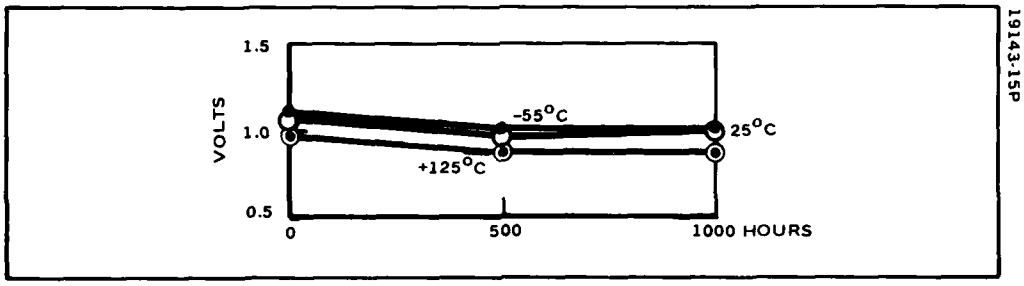



Figure 15. $V_{min}$ (0) for 2147 Suspect Devices

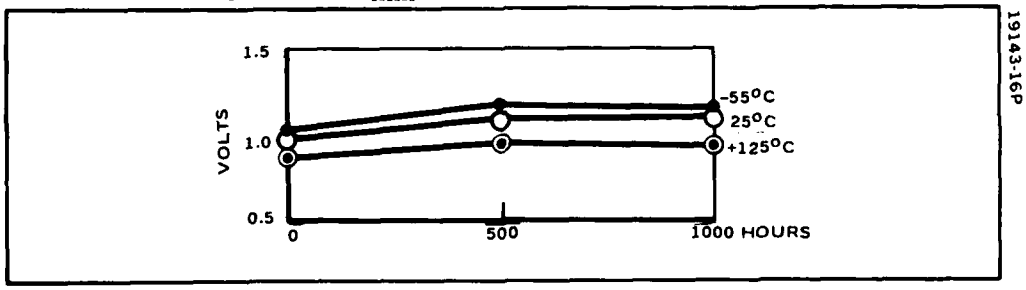



Figure 16. $V_{min}$ (0) for 2147 Non-Suspect Devices

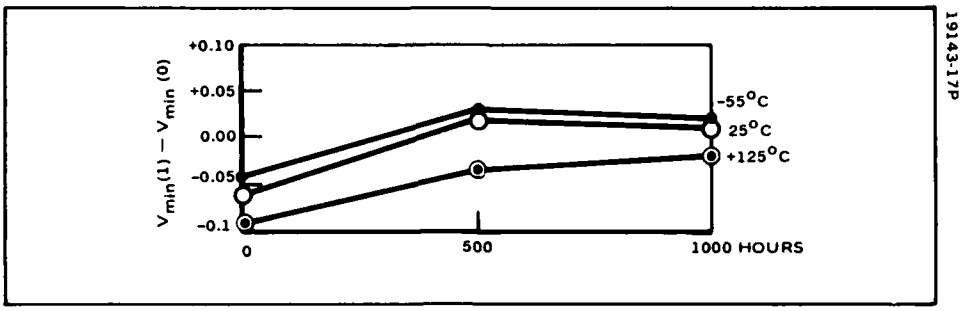



Figure 17. $V_{min}$ (1) – $V_{min}$ (0) for 2147 Suspect Devices

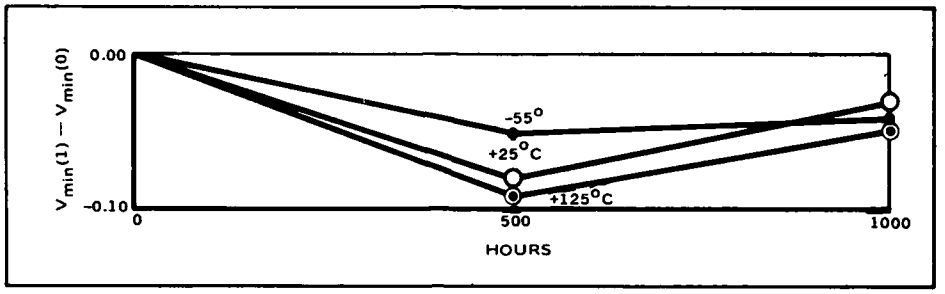



Figure 18. $V_{min}$ (1) – $V_{min}$ (0) for 2147 Non-Suspect Devices

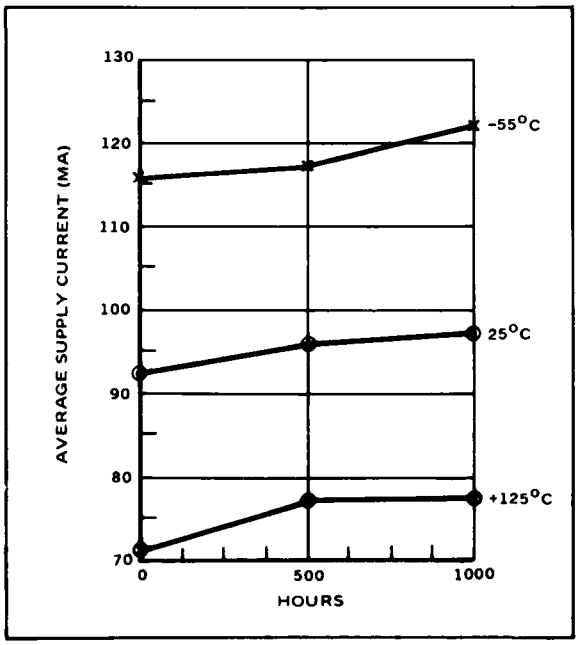



Figure 19. $I_{cc}$ for 2147 Suspect Devices

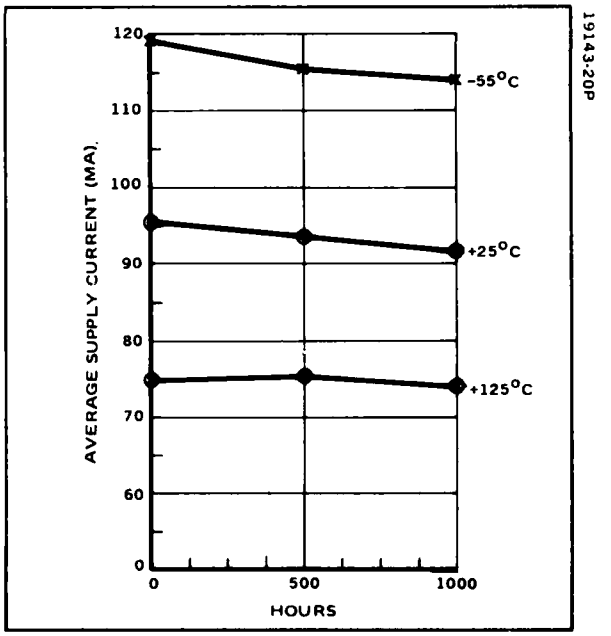



Figure 20. $I_{cc}$ for 2147 Non-Suspect Devices

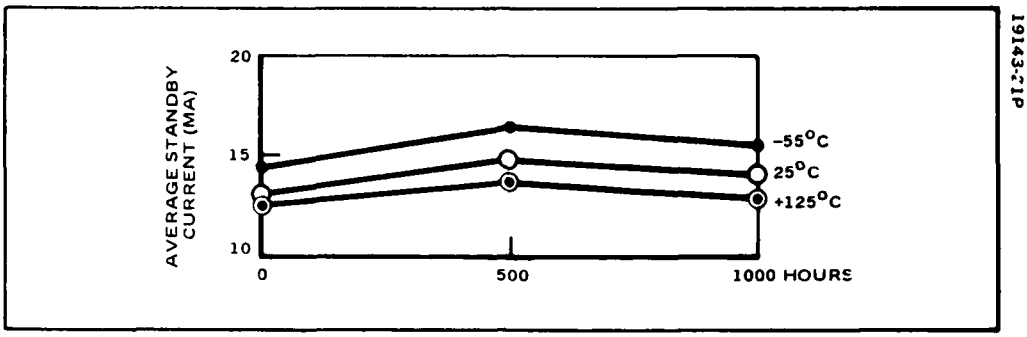



Figure 21. $I_{SB}$ for 2147 Suspect Devices

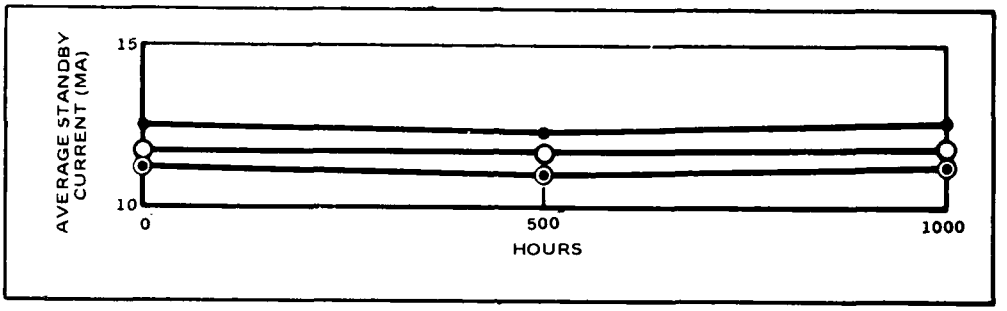



Figure 22. $I_{SB}$ for 2147 Non-Suspect Devices

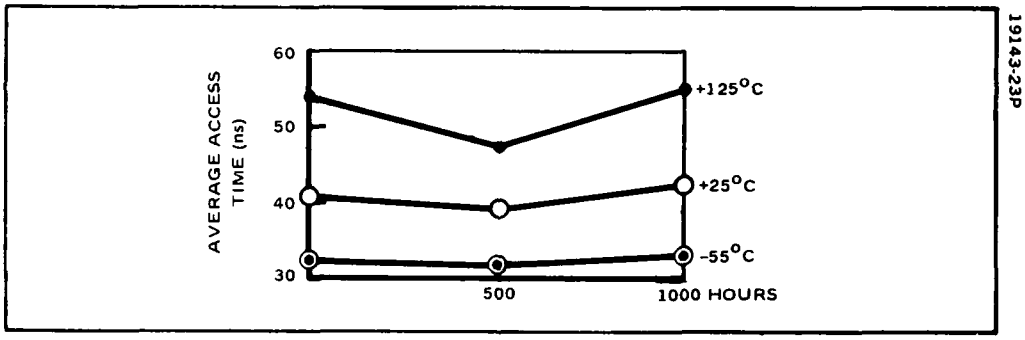



Figure 23. $T_{AA}$ for 2147 Suspect Devices

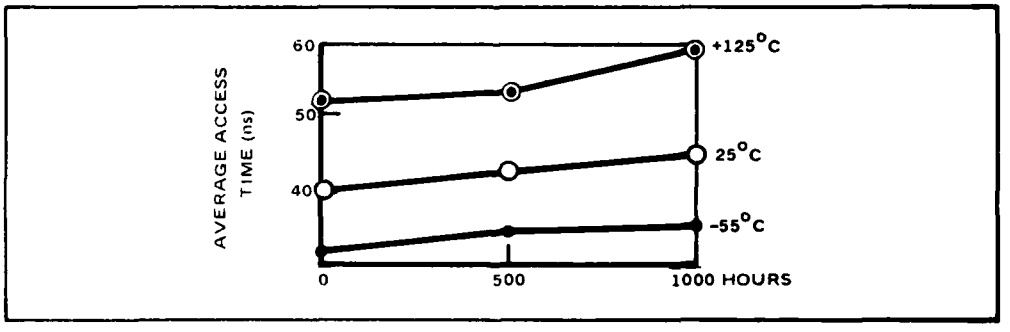



Figure 24. $T_{AA}$ for 2147 Non-Suspect Devices

## 2. LIFE TESTING OF DYNAMIC RAMs

Initial life tests of dynamic RAMs using the selected test parameters disclosed several devices not meeting specifications. Those parts that passed the special electrical tests did not exhibit any significant trend toward failure during the life test period, and the majority of those that had initial failure stayed as failure except for a few marginal cases.

A review of the life test data shown in Tables 8 through 10 indicates none of the devices failed or exhibited a trend towards failure except for those detected at the start of the life test program. Table 8 shows that at 85°C, suspect device 594S did not meet the 2 ms time requirement of the refresh test, and became worse by end of the life test. The TWCEH test found 11 parts that would not meet the specification limit of 4 μs maximum at 85°C at the start of the life test program. All TWCEH failures except two remained as rejects until the end of life. Those two parts, 260S and 359S, that passed the TWCEH were subjected later to a more sophisticated test that confirmed the parts as being rejects. This is discussed in more detail in the following paragraphs under TWCE. The V-BUMP test data shows initial life test rejects for all of the suspect parts except two. At the end of the life tests, all initial failures remained the same, and one additional failure occurred in the non-suspect device 229.

Table 9 shows the same tests as in Table 8, but with the test temperature set at 25°C. All devices passed the refresh time and V-BUMP tests except device 594S. All devices passed the TWCEH test except devices 627S, 659S and 480S.

Table 10 shows the same tests as in Table 8 but with the test temperature set at 0°C. All devices passed refresh and V-BUMP tests except device 594S. All devices passed the TWCEH test except device 659S.

Refresh Time (TREF) – Refresh time test parameters, plotted from data reduced in the Sentry computer, and shown in Figures 25 and 26, indicate relative stability through the 1500 hours of life tests. Figure 25 shows average refresh time of the suspect devices, while non-suspect device refresh times are shown in Figure 26. Both groups of devices exhibited good stability and no drift trends at 0°C and 25°C were evident. High-temperature refresh time data shows more difficulty in measurement repeatability due primarily to the extreme sensitivity of the device leakage parameter to small temperature variations. It should be noted that the 85°C refresh time data for the 500-hour period is abnormally low. This was caused by instrumentation problems that are more fully discussed in Appendix B, Accelerated Life Tests.

TABLE 8. DYNAMIC RAM SPECIAL TEST PARAMETER DATA SUMMARY (85°C)

| No. | Refresh in ms (1 ms min) | | | | TWCEH in µs (4 µs min) | | | | V-BUMP | | | | | | | | Supplier |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | Start | | 500 Hr | | 1000 Hr | | 1500 Hr | | |
| | Start | 500 Hr | 1000 Hr | 1500 Hr | Start | 500 Hr | 1000 Hr | 1500 Hr | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | |
| 1 | 178.0 | 42.8 | 99.5 | 162.0 | | | | | | | | | | | | | AMD |
| 2 | 112.0 | 27.1 | 58.6 | 96.0 | | | | | | | | | | | | | AMD |
| 3 | 140.0 | 31.8 | 77.5 | 127.0 | | | | | | | | | | | | | AMD |
| 4 | 115.0 | 24.0 | 63.3 | 86.9 | | | | | | | | | | | | | AMD |
| 5 | 74.0 | 22.4 | 42.8 | 68.0 | | | | | | | | | | | | | AMD |
| 6 | 77.0 | 16.1 | 35.0 | 63.0 | | | | | | | | | | | | | AMD |
| 8 | 112.0 | 24.0 | 44.4 | 65.8 | | | | | | | | | | | | | AMD |
| 9 | 99.0 | 19.3 | 41.3 | 64.8 | | | | | | | | | | | | | AMD |
| 206 | 27.1* | 11.4 | 19.3 | 36.6 | | | | | | | F | F | | | - | - | TI |
| 214 | 127.0 | 44.4 | 68.0 | 99.5 | F | F | F | F | | | | | | | | | TI |
| 219 | 64.0 | 20.8 | 31.8 | 55.4 | | | | | | | | | | | | | TI |
| 220 | 55.0 | 14.6 | 24.0 | 46.0 | | | | | | | F | F | | | - | - | TI |
| 227 | 24.0 | 9.8 | 13.0 | 22.4 | F | F | F | F | | | F | F | | F | - | - | TI |
| 229 | 17.7 | 8.3 | 11.4 | 14.6 | | | | | | | - | F | | F | - | F | TI |
| 708 | 49.0 | 22.4 | 22.4 | 30.3 | F | F | F | F | | | | | | | | | TI |
| 134S | 27.0 | 11.4 | 22.4 | 31.8 | | | | | | | F | - | | | - | - | AMD |
| 146S | 24.0 | 16.1 | 20.8 | 28.7 | | | | | | | | | | | | | AMD |
| 260S | 24.0 | 6.7 | 9.8 | 17.7 | F** | F | F | F** | F | F | F | F | F | F | F | F | TI |
| 263S | 8.28 | 3.6 | 5.1 | 67.1 | | | | | F | F | F | F | F | F | F | F | TI |
| 348S | 9.85 | 5.1 | 6.7 | 8.3 | F | F | F | F | F | F | F | F | F | F | F | F | TI |
| 359S | 8.28 | 3.6 | 5.1 | 6.7 | F** | F | | - | F | F | F | F | F | F | F | - | TI |
| 435S | 6.71 | 3.6 | 5.1 | 6.7 | | | | | F | F | F | F | F | F | F | F | TI |
| 470S | 8.28 | 3.6 | 5.1 | 6.7 | | | | | F | F | F | F | F | F | F | F | TI |
| 480S | 6.71 | 3.6 | 3.6 | 5.1 | F | F | F | F | F | F | F | F | F | F | F | F | TI |
| 493S | 6.71 | 3.6 | 5.1 | 6.7 | F | F | F | F | F | F | F | F | F | F | F | F | TI |
| 520S | 14.58 | 6.7 | 8.3 | 11.4 | | | | | F | - | F | F | F | F | F | - | TI |
| 594S | 1.66 | 0.7 | .35 | 0.8 | F | F | F | F | F | F | F | F | F | F | F | F | TI |
| 627S | 13.0 | 6.7 | 8.3 | 14.3 | F | F | F | F | F | F | F | F | F | F | F | F | TI |
| 659S | 14.58 | 5.1 | 6.7 | 11.4 | F | F | F | F | F | F | F | F | F | F | F | F | TI |
| 821S | 8.28 | 3.6 | 5.1 | 8.28 | | | | | F | F | F | F | F | F | F | F | TI |

S = Suspect F = Failure * = Data from No. 226 ** = Failure in map test

## 2. LIFE TESTING OF DYNAMIC RAMs (Continued)

TABLE 9. DYNAMIC RAM SPECIAL TEST PARAMETER SUMMARY (25°C)

| | Refresh (sec) | | | | TWCEH (4us min) | | | | V-BUMP | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| No. | Start | 500 Hr | 1000 Hr | 1500 Hr | St | 500 Hr | 1000 Hr | 1500 Hr | St | 500 Hr | 1000 Hr | 1500 Hr |
| 1 | 1.6* | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 2 | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 3 | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 4 | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 5 | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 6 | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 8 | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 9 | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| **206 | ** | 1.6 | 1.6 | 1.6 | ** | | | | ** | | | |
| 214 | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 219 | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 220 | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 227 | 0.21 | 0.20 | 0.42 | 0.22 | | | | | | | | |
| 229 | 0.35 | 0.33 | 0.34 | 0.29 | | | | | | | | |
| 708 | 1.6 | 1.4 | 1.2 | 0.81 | | | | | | | | |
| 134S | 0.10 | 0.10 | 0.13 | 0.12 | | | | | | | | |
| 146S | 0.12 | 0.11 | 0.11 | 0.146 | | | | | | | | |
| 260S | 1.6 | 1.2 | 1.2 | 1.41 | | | | | | | | |
| 263S | 0.15 | 0.14 | 0.15 | 0.146 | | | | | | | | |
| 348S | 0.17 | 0.16 | 0.16 | 0.171 | | | | | | | | |
| 359S | 0.13 | 0.13 | 0.14 | 0.134 | | | | | | | | |
| 435S | 0.11 | 0.10 | 0.10 | 0.10 | | | | | | | | |
| 470S | 0.14 | 0.13 | 0.14 | 0.14 | | | | | | | | |
| 480S | 0.10 | 0.10 | 0.10 | 0.10 | | F | F | F | | | | |
| 493S | 0.11 | 0.11 | 0.11 | 0.11 | | | | | | | | |
| 520S | 0.30 | 0.28 | 0.29 | 0.29 | | | | | | | | |
| 594S | 0.005 | 0.001 | 0.001 | 0.001 | | | | | F | F | F | F |
| 627S | 0.30 | 0.30 | 0.30 | 0.30 | F | F | F | F | | | | |
| 659S | 0.35 | 0.35 | 0.35 | 0.379 | F | F | F | F | | | | |
| 821S | 0.23 | 0.20 | 0.20 | 0.20 | | | | | | | | |
| **226 | 0.55 | - | - | - | | - | - | - | | - | - | - |

*1.6 seconds is maximum for this series of tests.
**226 was replaced by 206.

TABLE 10. DYNAMIC RAM SPECIAL TEST PARAMETER DATA SUMMARY (0°C)

| | Refresh (sec)** | | | | TWCEH (4usec min) | | | | V-BUMP | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| No. | Start | 500 Hr | 1000 Hr | 1500 Hr | St | 500 Hr | 1000 Hr | 1500 Hr | St | 500 Hr | 1000 Hr | 1500 Hr |
| 1 | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 2 | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 3 | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 4 | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 5 | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 6 | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 8 | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 9 | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| *226 | 1.6 | - | - | - | | - | - | - | | - | - | - |
| *206 | - | 1.6 | 1.6 | 1.6 | - | | | | - | | | |
| 214 | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 219 | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 220 | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 227 | 1.6 | 0.44 | 1.2 | 1.5 | | | | | | | | |
| 229 | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 708 | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 134S | 0.29 | 0.34 | 0.34 | 0.367 | | | | | | | | |
| 146S | 0.39 | 0.37 | 0.31 | 0.45 | | | | | | | | |
| 260S | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 263S | 1.6 | 1.6 | 1.2 | 1.6 | | | | | | | | |
| 348S | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 359S | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 435S | 0.81 | 0.81 | 1.71 | 0.16 | | | | | | | | |
| 470S | 1.56 | 1.51 | 1.41 | 1.6 | | | | | | | | |
| 480S | 0.61 | 0.59 | 0.55 | 0.61 | | | | | | | | |
| 493S | 1.2 | 1.2 | 1.1 | 1.6 | | | | | | | | |
| 520S | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 594S | 0.008 | 0.0016 | 0.0013 | 0.005 | | | | | F | F | F | F |
| 627S | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |
| 659S | 1.6 | 1.6 | 1.6 | 1.6 | F | F | F | F | | | | |
| 821S | 1.6 | 1.6 | 1.6 | 1.6 | | | | | | | | |

* = 226 was replaced by 206.

** = 1.6 seconds represents a self imposed upper limit made necessary by practical considerations of test time.

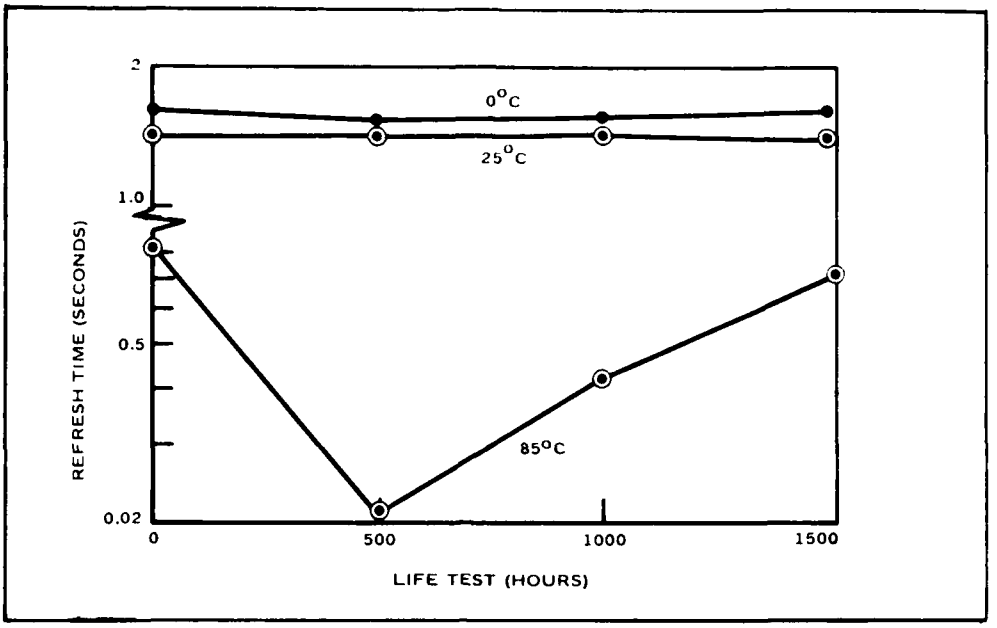



Figure 25. Refresh Time for 9050, 4050 Dynamic RAMs Suspect Devices. Low temperature data is stable but, high temperature data is marred by instrumentation error at 500 hours causing abnormally low readings.

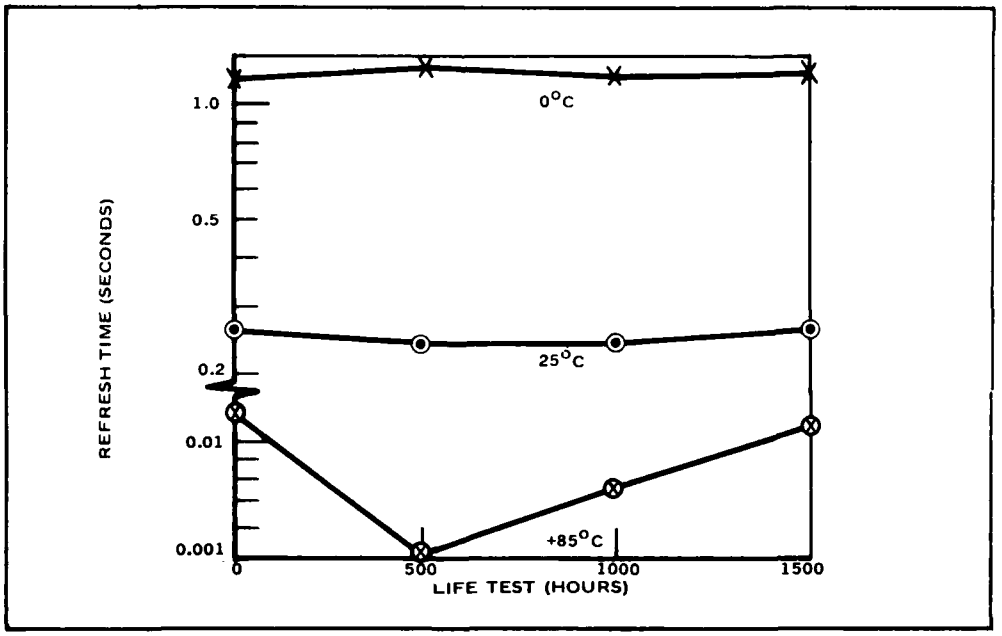



Figure 26. Refresh Time for 9050, 4050 Dynamic RAMs – Non-Suspect Devices. Low temperature data is stable but high temperature data is marred by instrumentation error at 500 hours causing abnormally low readings.

## 2. LIFE TESTING OF DYNAMIC RAMs (Continued)

Chip Enable Test (TWCE) – The go/no-go measurements to identify devices that are unable to sustain a long TWCE pulse are shown in Table 8. Quantized measurements from the memory mapping program are shown in Figure 27. Again, the low readings at 500 hours show the error due to the temperature probe.

The failure data for TWCE (in Table 11) could not be precisely assigned to TWCEH or TWCEL for the dynamic circuits, so results are lumped. A total of 9 TWCEH test rejects were noted when the tests were newly installed at the beginning of the life test program (see Table 8). Quantized TWCE data when retested during memory mapping showed two additional rejects for a total of 11. The test time is considerably longer when mapping is included. Thus, the devices reached higher junction temperatures. This is probably the reason two additional rejects were found. Figure 28 shows a basic Sentry timing diagram utilized for normal functional tests. The TWCE pulse widths have been set at minimum pulse width to allow maximum test speed. Figure 29 shows the method of determining the exact TWCEH pulsewidth at which failure occurs. The overall time period was fixed and the CE high pulse increased from minimum to maximum pulse width while searching for a failure value, while all other pulses remain as in Figure 28. The CE low period was decreased correspondingly. It was assumed that the dynamic circuits receive their precharge during the low period, and the most of the dynamic circuits are active when the CE pulse goes high. However, the test data indicates that both pulse periods may be critical and may be reacting to each other. It was decided to change the test program and retest the devices to determine which parameter was primarily responsible for the 11 TWCEH rejections.

When retesting for TWCEH, it was decided to keep TWCEL at a constant value (1 μs) and allow the cycle time period to vary (See Figure 30). Conversely, when testing for TWCEL it was decided to fix the TWCEH high pulse width at a conservative value (2 μs). This allowed minimum interaction between the test parameters and facilitated concentrating on evaluating one test parameter per test. In order to fully characterize the TWCEH and TWCEL parameters beyond the maximum specification limit of 4 μs, it was decided to extend the maximum to 100 μs.

Results of all devices rescreened with the new test procedure are shown in Table 11. Average TWCEL pulse width as a function of temperature is shown in Figure 31. The results were quite revealing in that all CE failures that were thought to be TWCEH failures were not due to the high pulse state. Over two thirds of the rejects could be attributed to failures caused by TWCEL not being able to meet the minimum pulse width low of 130 nanoseconds.

Table 11 shows the results of measuring TWCEL by keeping TWCEH constant at 2 microseconds. Out of 30 devices, 21 were unable to reach a minimum pulse width of 130 nanoseconds when required to hold TWCEH for 2 microseconds at 85°C. Figure 31 also shows that only at 25°C is the average TWCEL able to come close to meeting the 130-nanosecond requirement. It is understandable that failures occur at larger pulse widths at high temperature, but it is not obvious why failures increase at 0°C. More precharge time is required at high temperature probably due to boot-

TABLE 11. TWCE DATA FOR DYNAMIC RAMS – REVISED PROCEDURE

| No. | 1500 Hours | | | | | | Supplier | Original Failures |
|---|---|---|---|---|---|---|---|---|
| | 0°C | | 25°C | | 85°C | | | |
| | H | L | H | L | H | L | | |
| 1 | 100 | 0.06 | 100 | 0.06 | 100 | 0.06 | AMD | |
| 2 | | 0.63 | | 0.25 | | 0.80 | | |
| 3 | | 0.54 | | 0.15 | | 0.96 | | |
| 4 | | 0.62 | | 0.15 | | 0.70 | | |
| 5 | | 0.51 | | 0.23 | | 0.06 | | |
| 6 | | 0.61 | | 0.22 | | 0.72 | | |
| 8 | | 0.46 | | 0.06 | | 0.17 | | |
| 9 | | 0.73 | | 0.54 | | 0.29 | AMD | |
| 206 | | 0.88 | 100 | 0.06 | 100 | 1.1 | TI | |
| 214 | | 0.45 | 63 | 0.06 | 10 | 0.07 | | F |
| 219 | | 0.06 | 100 | 0.06 | 93. | 0.51 | | |
| 220 | | 0.06 | 100 | 0.06 | 100 | 1.2 | | |
| 227 | | 1.07 | 27 | 0.48 | 10 | 0.96 | | F |
| 229 | | 0.06 | 100 | 0.06 | 100 | 0.24 | | |
| 708 | | 0.64 | 42 | 0.32 | 9.7 | 0.06 | TI | F |
| 134S | | 0.06 | 100 | 0.06 | 100 | 0.89 | AMD | |
| 146S | | 0.52 | 100 | 0.78 | 100 | 0.64 | AMD | |
| 260S | | 0.24 | 100 | 0.06 | 14 | 0.70 | TI | F |
| 263S | | 0.06 | 100 | 0.06 | 100 | 0.82 | | |
| 348S | | 0.53 | 39 | 0.06 | 9.9 | 0.07 | | F |
| 359S | | 0.12 | 100 | 0.06 | 18.5 | 0.54 | | F |
| 435S | | 0.06 | 100 | 0.06 | 33 | 0.52 | | |
| 470S | | 0.06 | 100 | 0.06 | 44 | 0.07 | | |
| 480S | | 0.06 | 11 | 0.06 | 9.1 | 0.06 | | F |
| 493S | | 0.55 | 56 | 0.06 | 10 | 0.07 | | F |
| 520S | | 0.06 | 100 | 0.06 | 100 | 2.55 | | |
| 594S | 100 | 0.70 | 33 | 0.51 | 11.1 | 1.0 | | F |
| 627S | 42 | 0.06 | 10 | 0.06 | 8.6 | 0.06 | | F |
| 659S | 10 | 0.51 | 9.1 | 0.06 | 4.4 | 5.0 | | F |
| 821S | 100 | 0.06 | 100 | 0.06 | 100 | 1.0 | TI | |

S = Suspect Note: All measurements in microseconds.

## 2. LIFE TESTING OF DYNAMIC RAMs (Continued)

strap node leakage increase. Tables 9 and 10 show that at low temperature TWCEH is improved considerably over measurements at 85°C.

TWCEH failures of devices 214, 708, 348, 480, 493, and 627 are probably due to the poor performance during the active portion of CE, since the TWCEL pulse widths are good (TWCEL is good down to 70 nanoseconds).

Although TWCE pulse failures did not appear to be degrading, this test parameter is an excellent method of margin testing the bootstrap dynamic circuits.

V-BUMP Test – As shown in Table 8, at 85°C all of the suspect devices and some of the non-suspect devices failed the V-BUMP tests. Those devices in the non-suspect group had low refresh times and the dominant failure period was 500 hours, when the ambient temperature was higher than the preset 85°C. However, at room temperature and 0°C, all of the V-BUMP failures passed the test except for device 594. Therefore, the V-BUMP failures are highly temperature-dependent and directly related to low refresh times.

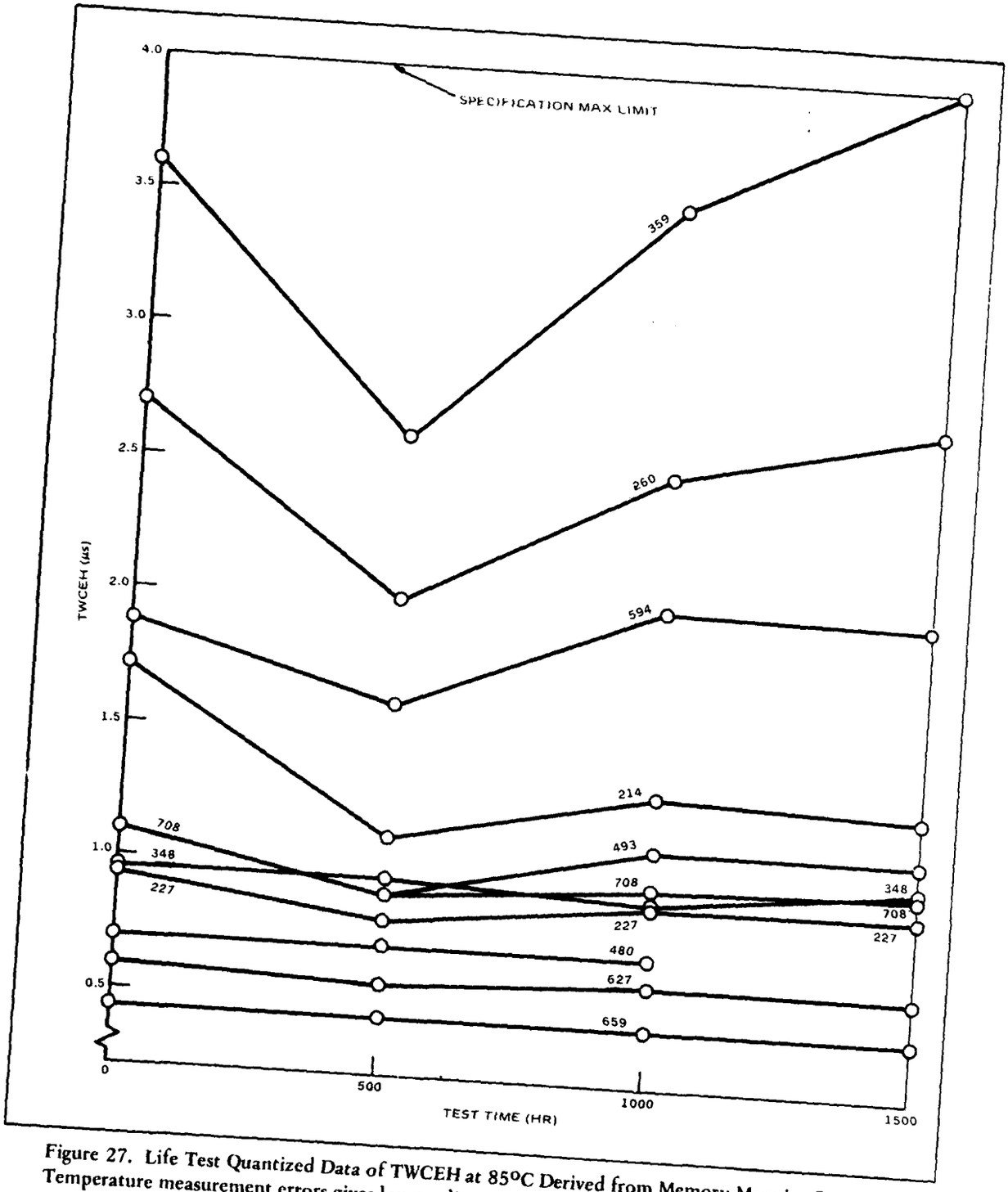



Figure 27. Life Test Quantized Data of TWCEH at 85°C Derived from Memory Mapping Program. Temperature measurement errors gives low readings at 500 hours.

2. LIFE TESTING OF DYNAMIC RAMs (Continued)

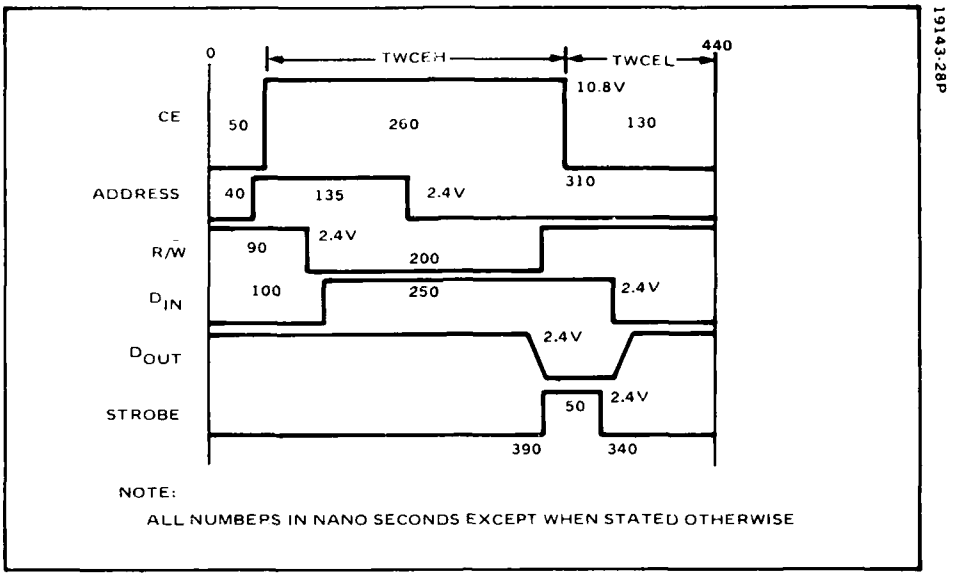



Figure 28. Typical Timing Waveforms – For All Standard Tests. TWCEH and TWCEL are set for minimum pulse widths to achieve maximum test speed.

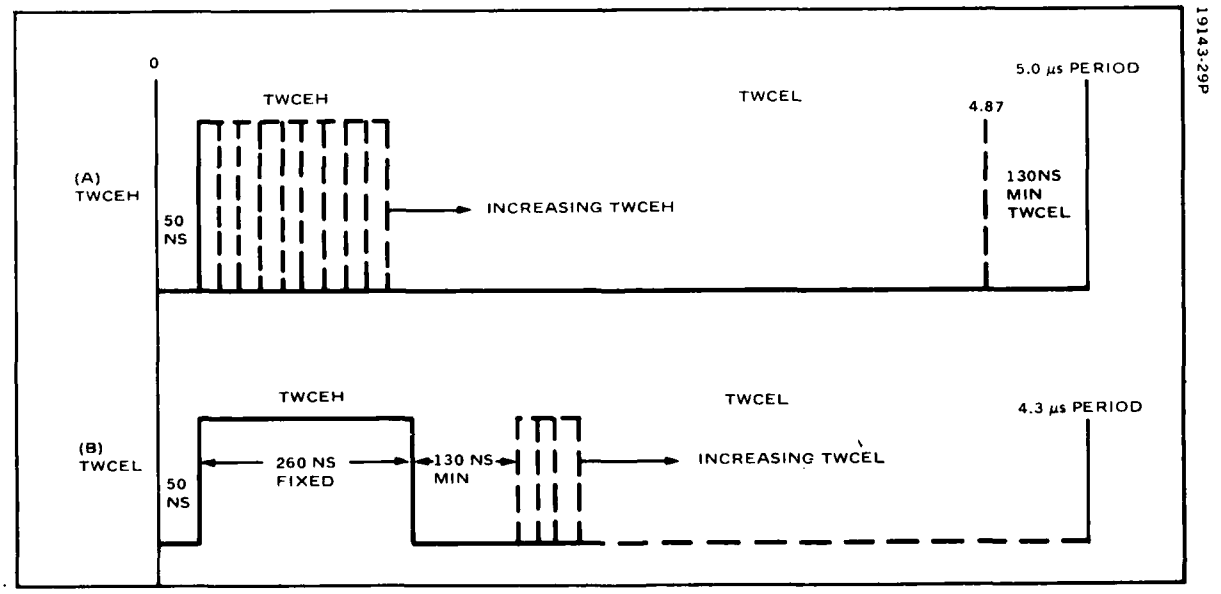



Figure 29. TWCEH and TWCEL Quantized Test Procedure. (A) TWCEH pulse width varies from 0 to 4.87 μs, (B) TWCEL varies from 130 NS to 4.3 μs.

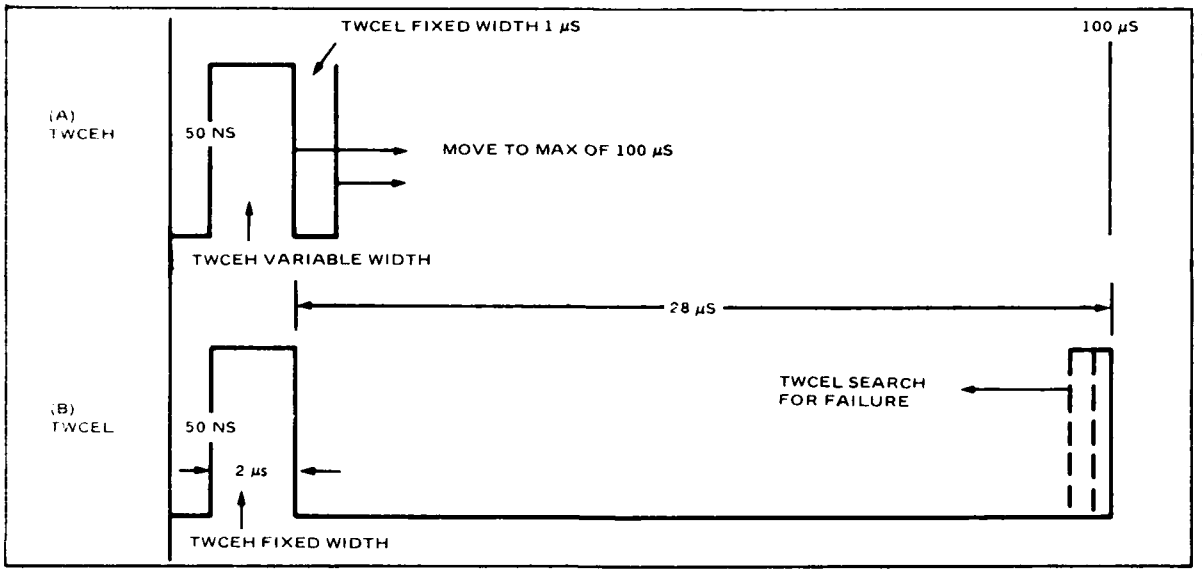



Figure 30. Revised TWCEH and TWCEL Quantized Test Procedure. (A) TWCEH varies from 0.26 μs to 100 μs, while TWCEL is constant at 1 μs. (B) TWCEL varies from 28 μs to 60 ns, while TWCEH is constant at 2 μs.

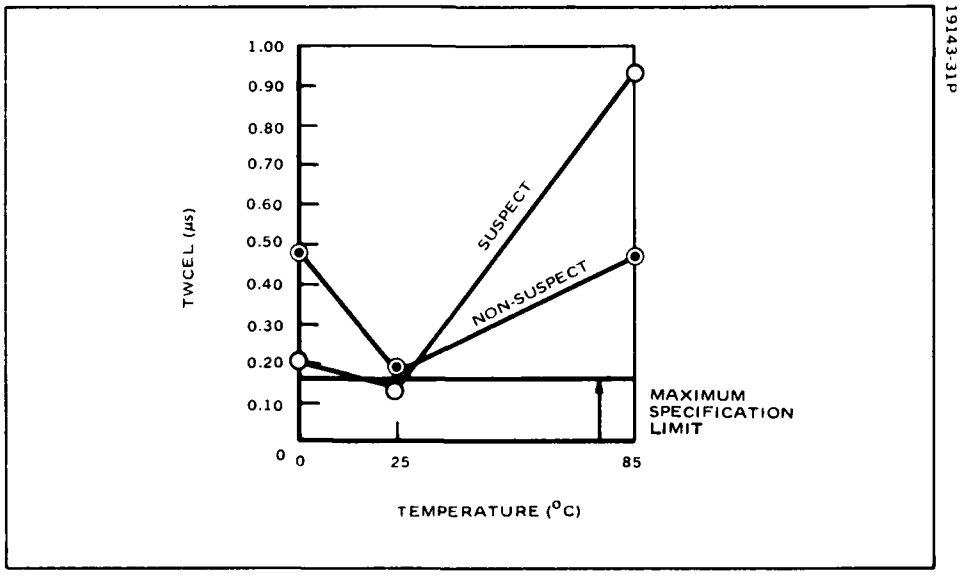



Figure 31. Electrical Characterization of TWCEL Test Parameter Under Revised Test Procedures. Data shows very poor performance at both low and high temperatures. Data was produced from devices after life tests were completed.

## SECTION 5
## FINDINGS

## 1. CONCLUSIONS AND RECOMMENDATIONS

The study and investigative efforts did not result in a viable LSI failure prediction test technique, but some excellent electrical screening methods were developed.

For static RAMs, the main test parameter investigated (the FF cell unbalance) did not prove to be a potential failure or reliability indicator, and can be generally disregarded as a useful test parameter except for two considerations. First, the test technique to detect FF cell unbalance may be an excellent alternative to the functional time-dependent failure (TDF) test technique. The TDF case was determined to be a special case of the cell FF unbalance phenomenon. Since TDF tests can take as long as 5 seconds to run, the unbalance test technique (Vmin), when used with high temperature stress, can detect potential TDF failures considerably faster. TDF devices have been detected by the FF cell unbalance test methods during this investigation and during other reported investigations. However, more evidence is needed to prove that this failure mode is prevalent in industry and needs to be detected and eliminated through a standard test procedure.

The second consideration is the effect of internal and external electrical noise on the cell unbalance parameter, which was not investigated during the study. Noise disturbance from the $V_{CC}$ supply line, along with internal noise generated by special test patterns should be investigated relative to their effect on FF cell unbalance.

Although none of the dynamic RAMs that tested good initially, failed during life tests or showed any failure trends, the three test parameters under investigation proved to be excellent tools for screening devices that must meet initial electrical parameter requirements. Two of the electrical test parameters, $T_{REF}$ and TWCE, are highly effective in measuring the quality of the physical parameter, back bias leakage. V-BUMP is an excellent tool for electrical margin testing of memory cell – sense amplifier read and write operations.

In order to be effective, the present requirements for refresh time must be measured at high temperatures because the refresh time parameter can easily vary by an order of magnitude between room temperature and 85°C. In addition, the temperature-dependent physical parameter (back-bias junction leakage current) is usually masked by other leakage phenomena at room temperature. If high temperature refresh time tests are not used, and if room temperature tests are an economic choice, then the test limit must be increased by several times in order to screen out potential failures that may occur at the higher temperatures.

The TWCE tests that are presently called out in the test specification procedures are necessary but inadequate. A much more effective test of the periphery circuits that use clocked dynamic circuits has been developed in this investigation and should be implemented. In particular, the test for maximum pulse width TWCEH and minimum pulse width TWCEL shows the relative ability of the bootstrap circuit to drive its loads with a minimum of precharge energy. Present tests do not check the sustaining drive capability margin of the amplifiers. The tests are fairly rapid and a good margin test of all dynamic periphery circuits in the memory can be made. Both the active high TWCEH and precharge low TWCEL test should be utilized in a manner similar to the test technique that was developed. All of the newer 64-K dynamic RAMs use dynamic circuits quite extensively.

If substrate bias voltage $V_{bb}$ and supply voltage $V_{dd}$ are both available, every effort should be made to include a V-BUMP test as a standard test technique. Margin testing of a sense amplifier Read operation is an excellent test tool for screening. If the substrate bias voltage is not available, the V-BUMP test is less sensitive, but still a good test, and should be implemented into MIL-M-38510. Writing should be done at low $V_{dd}$ and reading at high $V_{dd}$. If the polysilicon plate capacitor is not at $V_{dd}$ but at ground, the V-BUMP test is not practical.

TABLE 12. CONCLUSIONS AND RECOMMENDATIONS SUMMARY

- Static RAM cell unbalance test investigations were unsuccessful. However, further studies should be undertaken relative to effects of noise on cell unbalance.
- Functionally tested time-dependent failures can be detected by FF cell unbalance tests, which are recommended for use in device qualification tests.
- It is recommended that all refresh tests be done at high temperature. If room temperature tests must be used, refresh time requirement should be increased a factor of 5, or more.
- It is recommended that a CE high pulse of 4 μs and a low pulse of 0.16 μs be included as a test requirement in the specifications for dynamic RAMs.
- The V-BUMP test should be included in the dynamic RAM test specifications for these devices.

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# APPENDIX A
# TEMPERATURE STEP STRESS PROCEDURE AND RESULTS

## SUMMARY AND CONCLUSIONS

A time-temperature step stress plan was implemented to determine the optimum high temperature at which the accelerated life test could be run on the limited number of suspect 2147 static RAMs available. The time-temperature procedure indicated that the 2147 static RAMs fails to operate at 225°C, therefore, an ambient temperature of 200°C was selected for the life test plan.

For the dynamic RAMs, it was known that these devices had a much lower operating temperature limitation, due primarily to the refresh time requirement. It was decided that a simple functional failure versus temperature would be sufficient to select the life test temperature. Sample testing indicated that life test temperature should be limited to 150°C.

## 2147 STATIC RAM TESTING

Figure A-1 summarizes the time-temperature step stress procedure used to test the 2147 static RAMs.

The stress test on a limited number of devices with known FF cell off-balance output nodes, and a set of reference devices with output nodes within the normal distribution, was initiated with the temperature set at 100°C for 168 hours. The temperature was raised in 50°C increments until a definite cell "unbalance" parameter degradation or failure occurred. If either device degradation or failure occurred then a larger sample life test plan was automatically triggered so that a meaningful reliability test was started and performed.

Figure A-2 shows the test configuration with which the stress test was performed. All inputs were in the high voltage reverse bias condition, except for the control inputs, WE, and data inputs. In order to set the output in the proper state, a Write operation was performed with a toggle switch and then a Read operation was set. All chips were controlled and set up in parallel, including the memory addresses, when the devices were mounted on a board and installed in an oven.

All of the devices had initial worst-case FF cell unbalances as shown in Table A-1.

The majority of the 2147 memories had basic FF unbalance voltages under 1.200 volts. The three suspect devices shown in the table had unbalances that show up slightly out of the distribution at 25°C, and appear more dramatically at 125°C.

The stress test to determine the accelerated life test operating temperature reached 225°C (see Table A-2). Two functional failures and one $V_{OL}$ failure occurred. Test data analysis of the functional failures show that they are not catastrophic. Serial # 281 had all DC parameters and functional tests at -55°C and +25°C okay, but fails functionally at +125°C. Schmoo plots indicate it will pass functionally if $V_{CC}$ is at +5.5V. Serial # 215 operates at -55°C but fails functionally at +25°C and +125°C. DC input/output leakages are okay, but the standby current and $I_{CC}$ are excessive, indicating probably internal function deterioration of one or more of the devices.

Since device problems and failures occur at 225°C, it was decided that any life test plan should not use a temperature stress exceeding 200°C.

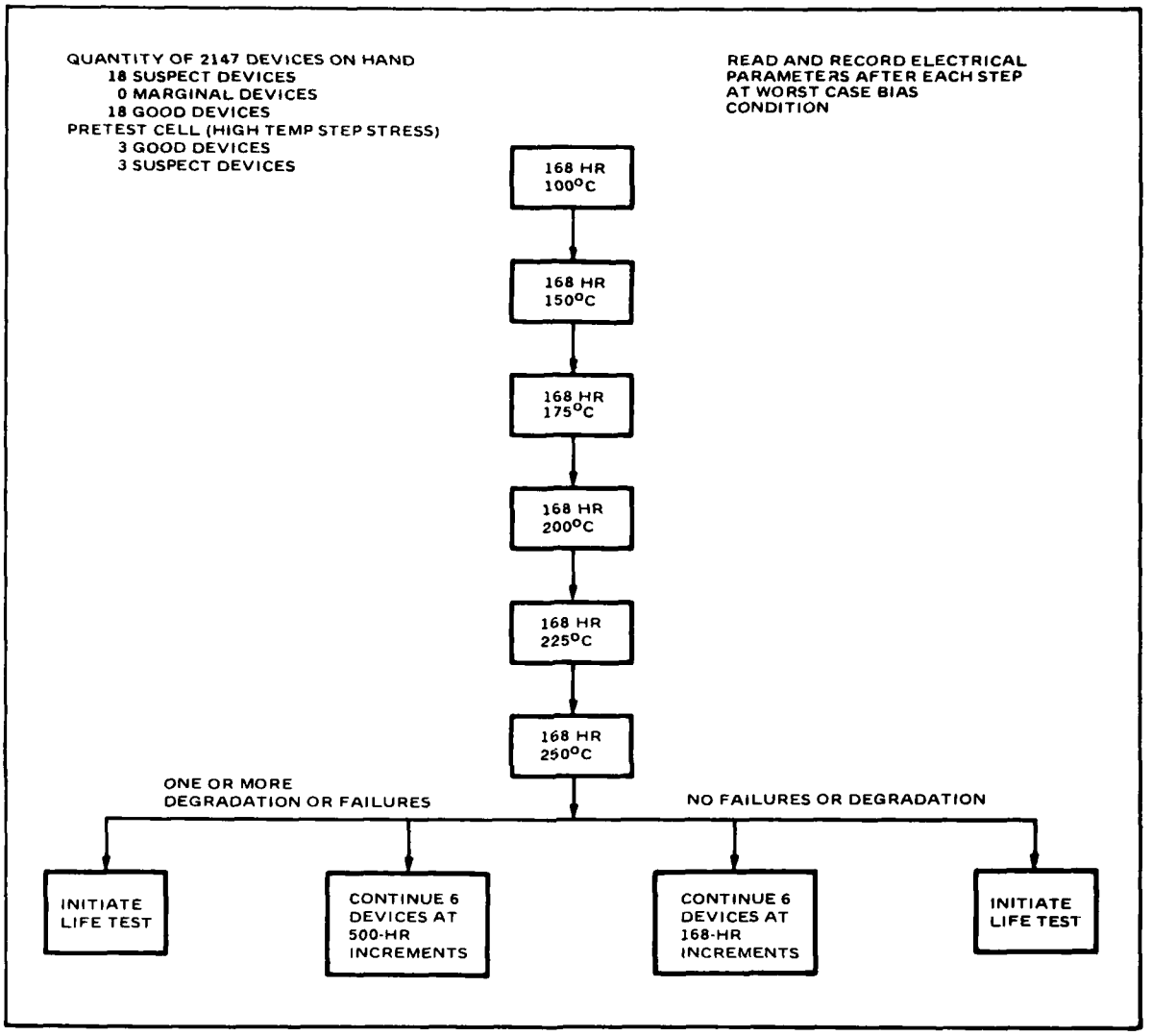


Figure A-1. Temperature Steps Stress Plan

TABLE A-1. INITIAL FF CELL UNBALANCE FOR THE 2147 MEMORY

| | Serial No. | Vendor | FF Offset at 25°C | | FF Offset at 125°C | |
|---|---|---|---|---|---|---|
| | | | 1 | 0 | 1 | 0 |
| Ref (1) | 102 | Intel | 0.998 | 1.098 | 0.698 | 1.098 |
| Devices (2) | 273 | Intersil | 0.898 | 0.998 | 0.598 | 0.698 |
| (3) | 281 | Intersil | 0.898 | 0.998 | 0.498 | 0.498 |
| Suspect (1) | 261 | Intersil | 0.998 | 1.498 | 0.698 | 3.699 |
| Devices (2) | 253 | Intersil | 1.098 | 1.098 | 1.798 | 2.198 |
| (3) | 215 | Intersil | 0.698 | 1.498 | 0.498 | 2.899 |

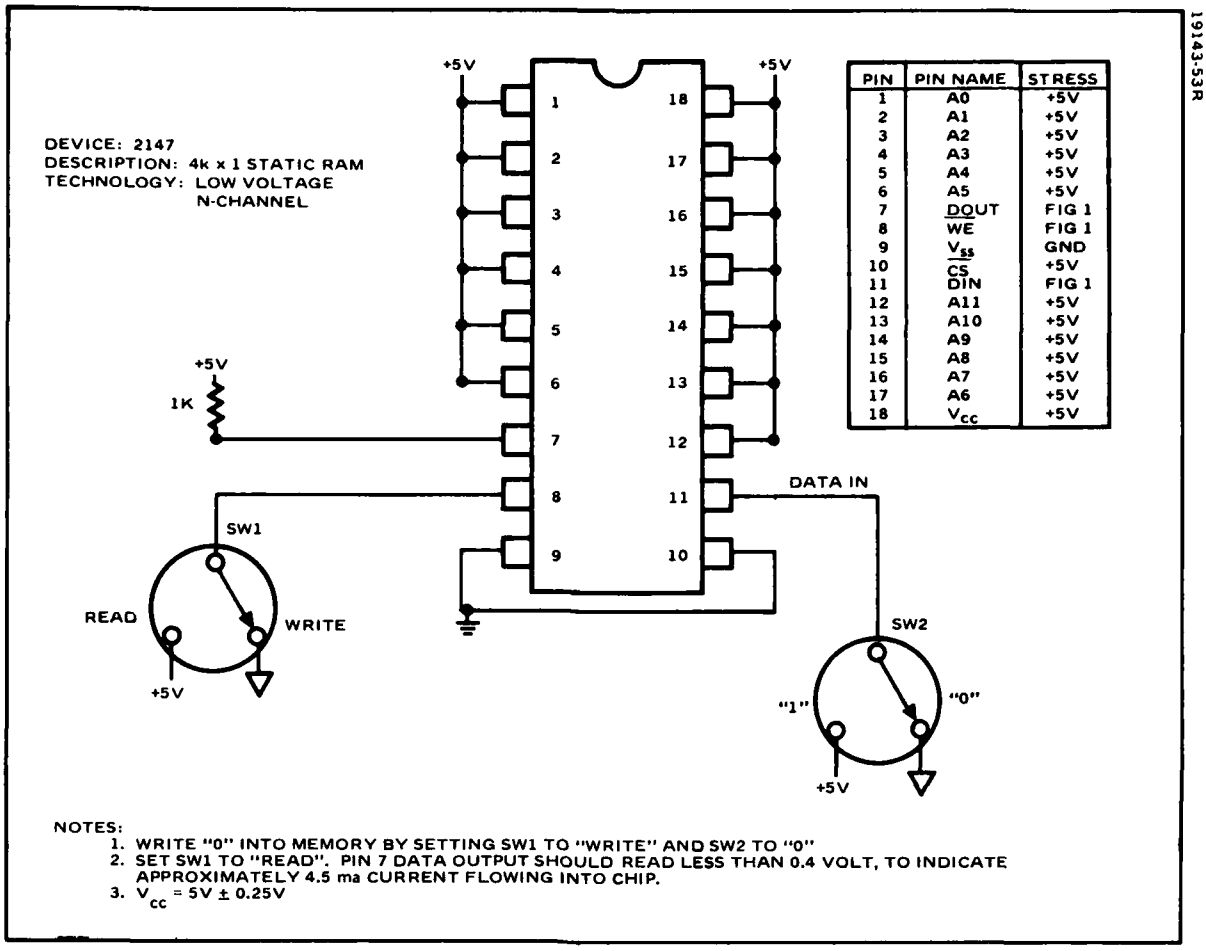


Figure A-2. Stress Test Configuration

TABLE A-2. 2147 STRESS TEST RESULTS

| Cum Test Time (hr) | Test Time (hr) | Temp (°C) | Good Parts | | | Suspect Parts | | |
|---|---|---|---|---|---|---|---|---|
| | | | No. 102 | No. 273 | No. 281 | No. 215 | No. 253 | No. 261 |
| 168 | 168 | 100 | OK | OK | OK | OK | OK | OK |
| 336 | 168 | 150 | OK | OK | OK | OK | OK | OK |
| 504 | 168 | 175 | OK | OK | OK | OK | OK | OK |
| 672 | 168 | 200 | 1/ | OK | – | – | OK | 2/ |
| 840 | 168 | 225 | – | – | Fails | Fails | – | – |

1/ $V_{IL}$ Marginal at 125°C

2/ $V_{OL}$ Fails at 25°C, OK at 125°C

## 9050 DYNAMIC RAM TESTING

A test investigation was launched to determine as quickly as possible the highest accelerated life test operating temperature that could be used. Table A-3 shows a matrix of 5 sample devices that indicate the temperature values in centigrade at which devices pass or fail a particular test parameter, using standard automatic test procedures.

Since the refresh time requirement is a predetermined value, higher operating temperatures can be used if refresh times are shortened from 2 milliseconds to a value approaching 32 microseconds. The 32 microseconds is the fastest rate at which this memory can be refreshed. V-BUMP testing represents worst-case voltage conditions, since both V-BUMP "0" and V-BUMP "1" tests were utilized. During these worst-case voltage conditions, access time measurements are made utilizing a checkerboard test pattern. A look at the table shows that worst-case V-BUMP test failures can occur as low as 85°C.

TABLE A-3. 9050 STRESS TEST INVESTIGATION

| Serial No. | Supplier | Type of Test | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Refresh | | V-BUMP | | Functional | | DC | |
| | | P | F | P | F | P | F | P | F |
| 156 | AMD | 105° | 115° | 95° | 105° | 160° | – | 160° | – |
| 159 | AMD | 105° | 115° | 95° | 105° | 135° | 140° | 145° | – |
| 161 | AMD | 95° | 105° | 95° | 105° | 155° | 160° | 160° | – |
| 450 | TI | 105° | 115° | 85° | 95° | 145° | 150° | 150° | – |
| 454 | TI | 105° | 115° | 75° | 85° | 150° | 155° | 155° | – |

P = Pass
F = Fail

On the other hand, the functional tests were operated with nominal voltage conditions, and these parts did not have any failures at the temperatures tested for V-BUMP. Since functional testing is most important for life tests, the temperature values attained in Table A-3 were utilized for determining the life test temperature. It was decided that 150°C was the upper limit for running life tests on these dynamic RAMs.

# APPENDIX B
# ACCELERATED LIFE TEST

## SUMMARY AND CONCLUSIONS

Accelerated life tests of both the 2147/7147 MOS static RAMs and the 9050/4050 MOS dynamic RAMs were performed to determine the stability of the selected test parameters of each type of RAM. Details of the exact life test procedures and conditions were defined.

The static RAMs had a number of failures, but none was attributed to the test parameters of interest (flip-flop cell off balance). After 1000 hours of static bias life tests at 200°C, the flip-flop cell unbalance parameters showed no evidence of failures.

The dynamic RAMs were subjected to a dynamic test for 1500 hours at 150°C ambient stress temperature. None of the three test parameters of interest showed failures, and no functional or parametric failures occurred.

## STATIC RAM TESTING

Fifteen samples of suspect flip flop (FF) unbalance devices and 15 samples of good devices were life tested. The test conditions were all address inputs and outputs floating, since it was decided that input/output devices should not influence reading the memory cells. The control input for device selection and read operating mode were set true. $V_{cc}$ was set to 5.0 ±0.5 volts nominal since protective series resistors were utilized for each device.

From a statistical viewpoint, conducting a 500-hour life test at 200°C on 30 devices is equivalent to 102 devices at 125°C for 1000 hours. Thirty static RAM test vehicles were tested at the 200°C stress condition.

The accelerated static life test for the static RAMs was started on March 10, 1981. Figure B-1 shows the test conditions and block diagram for this test. Previous high temperature step stress studies have shown that these devices can be life tested at 200°C with the power on and in a static state. Selected series resistors for each device were installed in the $V_{cc}$ lines external to the oven, so that none of the devices could destroy itself if a power latch-up condition occurred.

A plot of $I_{cc}$ current and device power dissipation is shown in Figure B-2. The device was limited to a maximum of 400 milliwatts and a short circuit current of 200 mA. The pin for $V_{dd}$ on each device was monitored daily so that any indication of abnormal voltage conditions could be determined in a timely manner. During the second week of the life test, a relatively high voltage was noted on one of the devices. This meant that the $V_{dd}$ line to the device under test was conducting less than normal current. A decision was made to turn power off and physically inspect

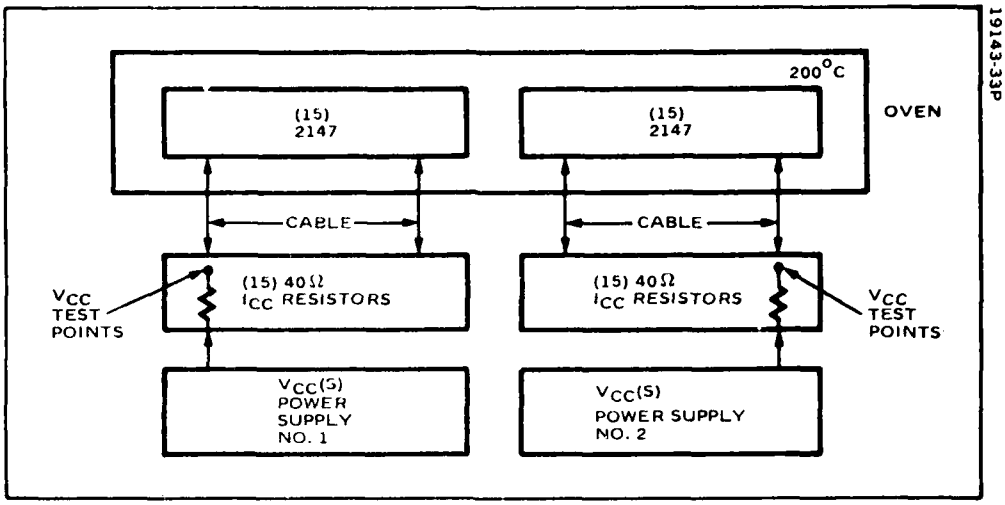


Figure B-1. 2147 Block Diagram of Static RAM Life Test.

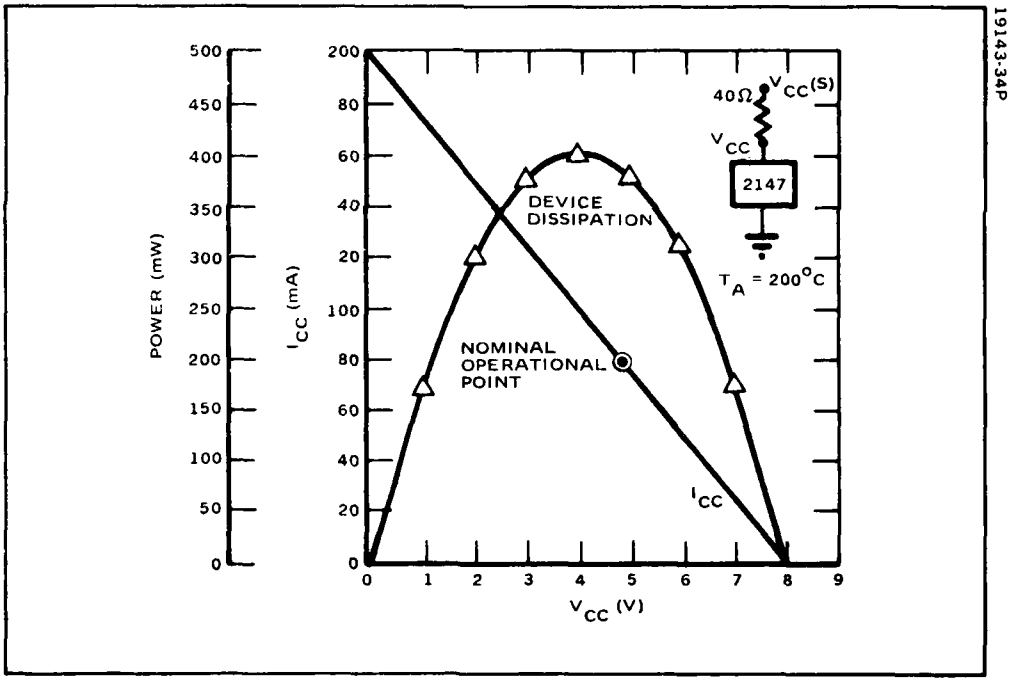


Figure B-2. 2147 Power Dissipation and $I_{CC}$ with 40-Ω Series Resistor.

the device for possible loss of contact at the socket pin or a poor solder connection. It turned out to be the latter, since the wire leading from the outside resistor to the device socket pin had fallen off. The device was immediately electrically tested on the Sentry ATE and verified as being good. The part and wire were reinstalled and the life test resumed immediately, all within a 1-hour period.

DATA at 500 Hours of Life Test – The 500-hour point for the life test on the 2147 devices was completed on March 31, 1981. Test data was taken during the next 24-hour period and the results analyzed. Seven devices appear to have failed either functionally or parametrically (see Table B-1). It should be noted that six out of seven failed were suspect devices. Initial reaction was that correlation between suspect device parameters and failures was indicated. Later physical failure analysis of the failures indicated this was not true. Those three devices that failed functional and AC parametric tests at all temperatures did not exhibit DC leakage failures at the output pin or any of the input pins. There was a definite loss of control at the output pin as shown in Table B-2, a matrix of output levels for VOH and VOL test conditions at three different temperatures. A program of physical failure analysis was performed on these three devices which included observation using a voltage contrast method on a scanning electron microscope (SEM). The results of the SEM analysis are discussed later.

TABLE B-1. 2147 PRELIMINARY ANALYSIS (AFTER 500 HR)

3 devices failed functions at all temperatures

No. 132(c), No. 266(s), No. 271(s)

2 devices failed functional at +125°C

No. 101(s), No. 265(s)

2 devices failed parametric tests

No. 131(s) input leakage 10.6 μA, S/B 10.0 μA maximum
No. 267(s) failed Taa

(c) = control, (s) = suspect, s/b = should be

TABLE B-2. 2147 FAILURE CHARACTERISTICS AT OUTPUT PIN

| Device No. | 25°C | | | -55°C | | | +125°C | | |
|---|---|---|---|---|---|---|---|---|---|
| | VOL | VOH | IOL | VOL | VOH | IOL | VOL | VOH | IOL |
| 132 | 2.046 | 1.52 | 0 | 2.046 | 2.5 | 0 | 1.56 | 1.03 | 0 |
| 266 | 2.046 | 0.95 | 0 | 2.046 | 1.3 | 7.5ua | 0.244 | 0.02 | 0 |
| 271 | 2.046 | 1.47 | 0 | 2.046 | 2.19 | 7.8ua | 2.046 | 0.82 | 0 |

A preliminary review of the FF cell unbalance characteristics was made. Figure B-3 shows a typical FF cell characteristic, Vmin, as a function of temperature. Vmin is defined as the $V_{CC}$ voltage at which the worst-case FF cell changes state to its natural state when it has been previously placed in the opposite state. A Vmin(1) indicates the minimum $V_{CC}$ voltage level required before the worst case FF cell changes state from a DATA true state to a $\overline{\text{DATA}}$ false state. A Vmin(0) indicates the minimum $V_{CC}$ voltage level required for the worst case FF cell to change state from $\overline{\text{DATA}}$ state to a DATA true state.

All three devices showing complete functional failures were removed from further life test. Testing was resumed with the remaining 27 devices. The 1000-hour point was reached on April 22, 1981, at which time the testing was concluded and final data taken.

It should be noted that the worst-case states, Vmin(1) or Vmin(0), do not always occur in the same memory cell. Memory cell mapping will indicate which cell or group of cells exhibit the worst-case minimum $V_{CC}$ voltage level.

In general, FF cells change state at the threshold point (Vt) of the transistors. Therefore, it is expected that the FF cell's changes follow the temperature characteristics of a MOS transistor threshold Vt. The Vt of MOS transistors have a negative temperature coefficient of about 3 mV per degree centigrade of temperature change (Reference 9).

From room temperature to +125°C, most of the FF cells showed typical state change characteristics (see Figure B-3). However, it was noted that some of the FF cells showed an unusual positive temperature characteristic (see Figures B-4 and B-5). Device No. 267 did not fail at 500 hours, but devices No. 266 and No. 271 did. There was no clear indication at the time that the failures could possibly be linked to these unusual characteristics. It should be noted that the so-called "suspect" devices were selected on the basis of a high Vmin value (above 1.4 volt) or a large unbalance value (at least 0.5 volt).

Data at 1000 Hours of Life Testing – The 1000-hour point for the life test of the 2147 devices was completed on April 22, 1981. A total of 10 failures was record d, including those tested at 500 hours (see Table B-3). Three of the parts that previously showed marginal parameter failures at 500 hours have now passed their tests, and they are serial numbers 131, 265 and 101. Moisture condensation problems on the parts at -55°C often create erroneous readings, in particular for low leakage currents measurements. The first two parts had marginal leakage failures at -55°C but were okay at other temperatures, so these parts were probably good at the 500 hour point. Device #101 previously had failed two out of six different functional test patterns at +125°C only. All DC tests were okay. Subsequent testing has not been able to repeat this failure, and therefore it was assumed that a poor or momentary contact problem had occurred during the 500 hour test for this particular device. Those ten devices that failed were distributed between six suspect and four non-suspect devices. Failure analysis, using

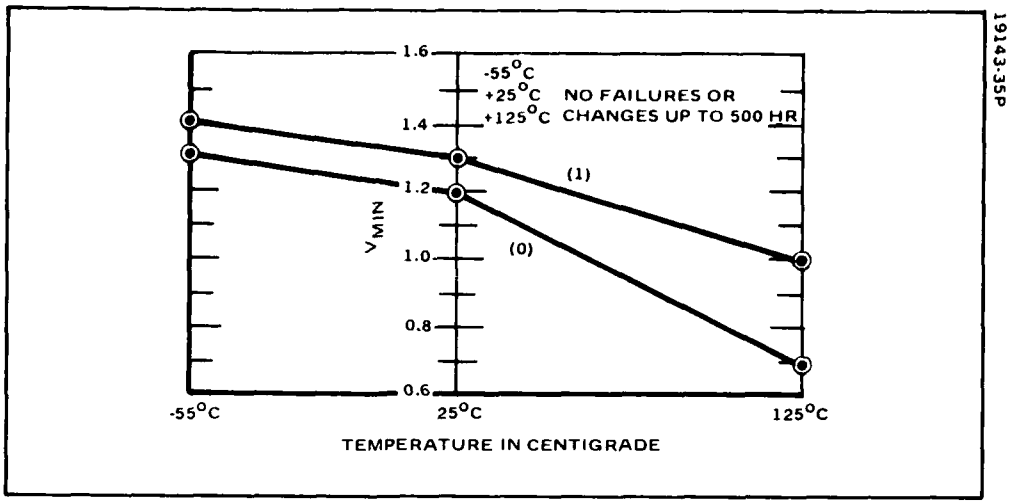


Figure B-3. 2147 $V_{min}$ vs Temperature -- No. 267 (Suspect)

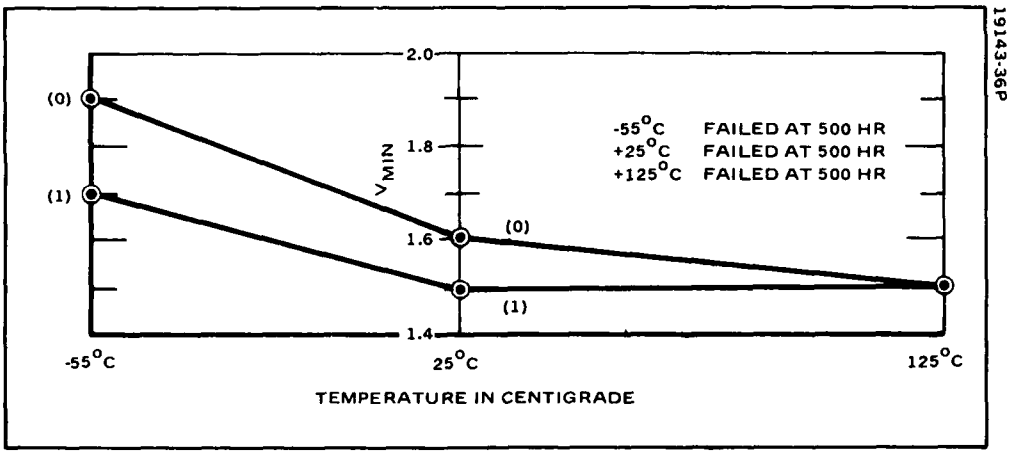


Figure B-4. 2147 $V_{min}$ vs Temperature – No. 266 (Suspect).

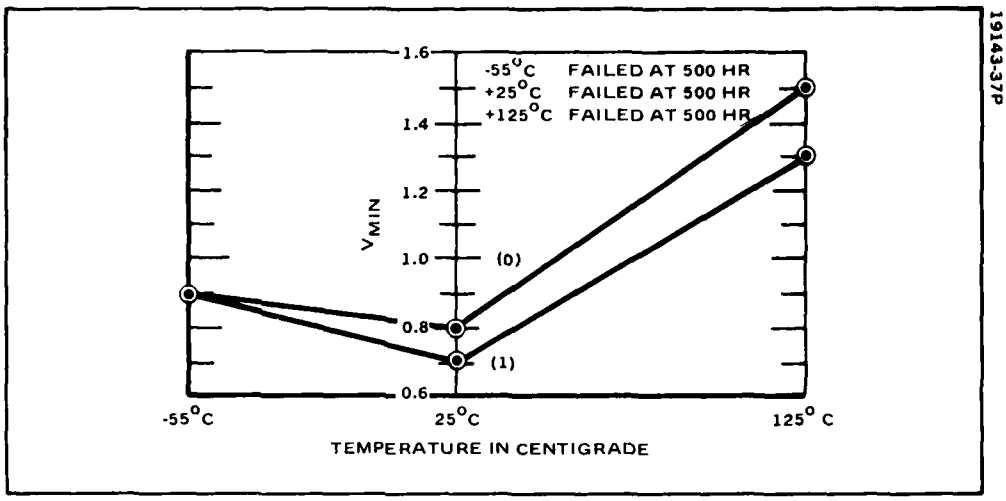


Figure B-5. 2147 $V_{min}$ vs Temperature -- No. 271 (Suspect).

TABLE B-3. 2147 ACCELERATED LIFE TEST SUMMARY

A. Test Conditions

- Static Power (365 mW)
- 200°C Ambient Temperature
- 1000 Hours, 30 Devices
- 30 Devices (13 Intel, 17 Intersil)

B. Failure Analysis

- 6 Suspect Devices
- 4 Non-Suspect Devices
- All Intersil Failures
- 8 Functional and Parametric Failures
- 2 Partial Functional Failures

a SEM shows that the functional failures at 500 and 1000 hours were caused by an aluminum conductor open on the $V_{CC}$ line as shown in Figures B-6, B-7, and B-8. The open lines were caused by aluminum electromigration as delineated in Table B-4. Although the most ovious failure occurred from metal electromigration as shown in the SEM photo, the silicon migration was also considered. However, silicon migration would create pits in the contact area and is not as easily confirmed. The accumulation of aluminum as hillocks is shown in Figure B-9 in the contact area. Apparently, aluminum migration can occur through silicon as well as aluminum, therefore voids and hillocks need not occur on the same metal line (Reference 10). Figure B-10 shows that in an unstressed control device, the metal deposition dropping into the contacts appears to be normal, and no excessive thinning of the metal occurs at the contact edges, although actual cross sectioning of the contact should be made to varify this. Figure B-11 shows that voids are appearing in other areas of the memory, including the cells.

TABLE B-4. 2147 FAILURE ANALYSIS

- Primary failure was due to electromigration
- Voids and hillocks occurred on contacts
- Electromigration voids occurred all over the chip as a function of voltage stress
- Probable cause - poor aluminum metal processing and/or metal composition

It is quite apparent that these devices have a critical electromigration problem that must be more thoroughly investigated. EDAX measurements indicate that the aluminum appears to be almost pure, with traces of silicon. The vendor verified that the aluminum should have 1% silicon. Actual current density has not been measured, but calculations based on certain assumptions (see Figure B-12) indicate that the maximum current density can be easily exceeded depending upon how much current actually flows in each of the four main branches from the $V_{CC}$ input pad. The $V_{CC}$ line in which the opens occur is 13 microns wide. The voids in the contact areas are following grain boundaries, and therefore nonuniform grain boundaries appear to be one of the contributing problems (references 10 and 11).

Intersil has stated that they are not aware of any metallization problems, but that they have not done any high temperature (over 125°C) accelerated life tests. However, the following information was received from them:

- Evaporated aluminum is deposited to approximately 1 micron thickness
- Aluminum has 1% silicon
- No metal barriers were used under the aluminum in the contacts
- Design current density is to an industry standard 1-mA/micron width
- Intersil has seen no electromigration during the 125°C, 1000-hour life test for the 7147.

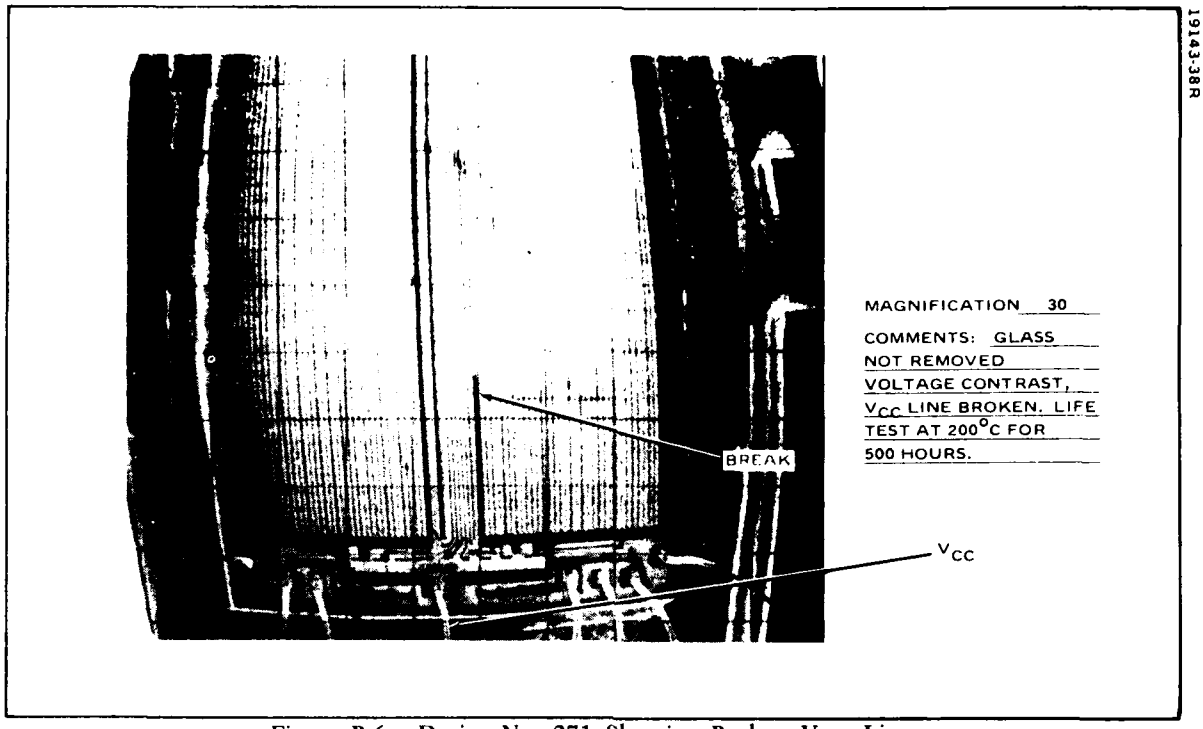


Figure B-6. Device No. 271 Showing Broken $V_{CC}$ Line

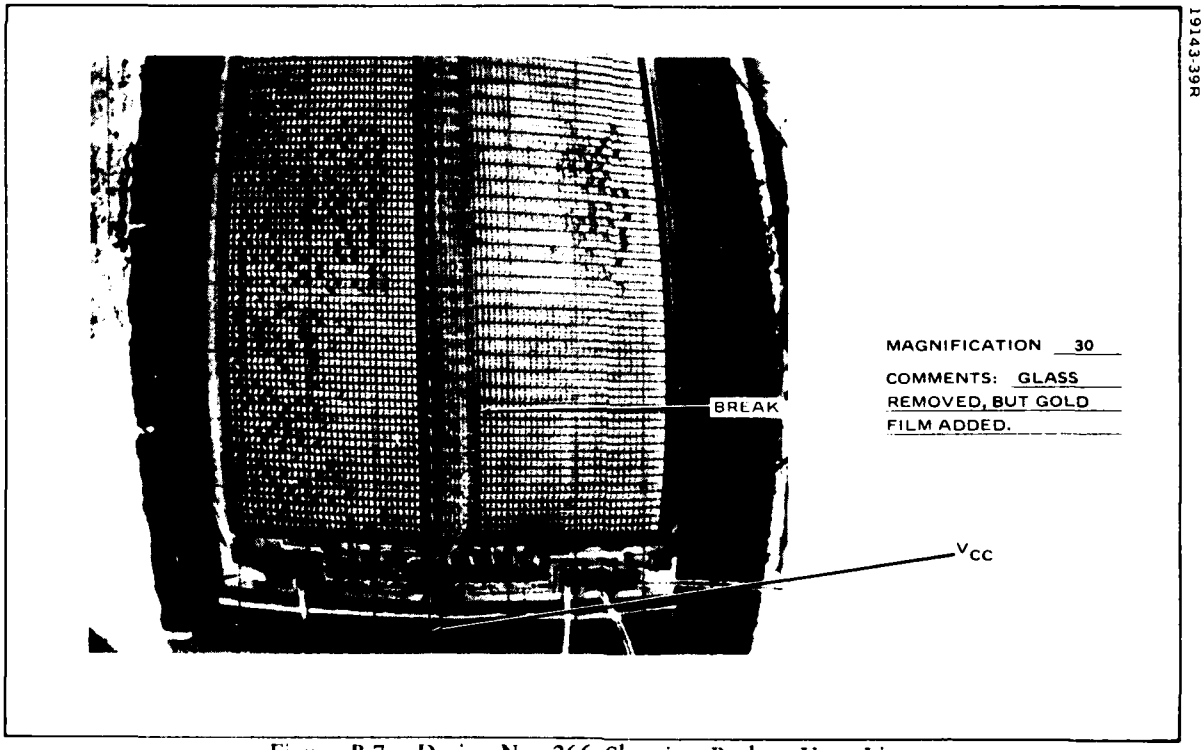


Figure B-7. Device No. 266 Showing Broken $V_{CC}$ Line

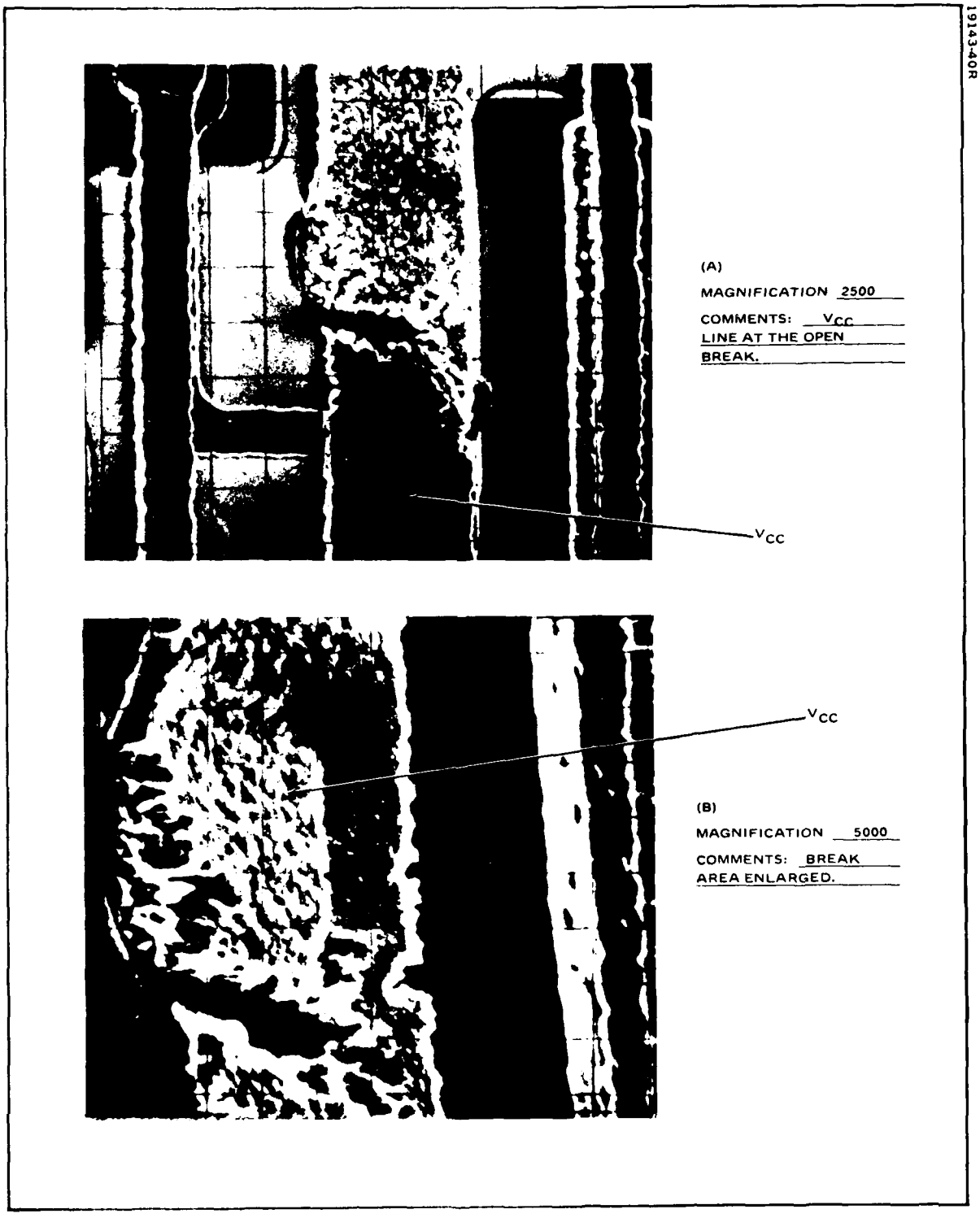


Figure B 8. SEM Photographs of Device No. 266 Showing Enlargements of $V_{CC}$ Break

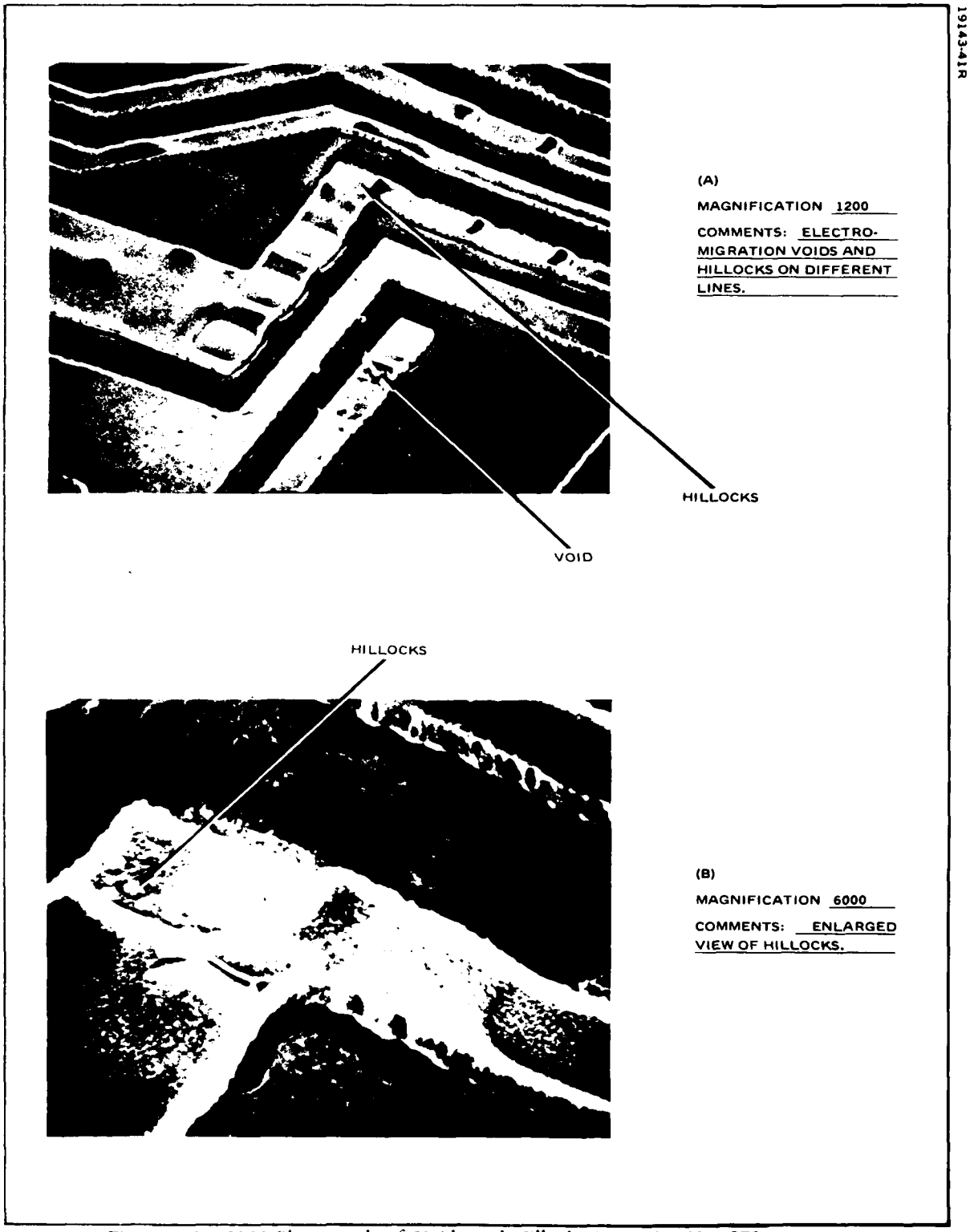


Figure B-9. SEM Photograph of Voids and Hillocks in Device No. 271

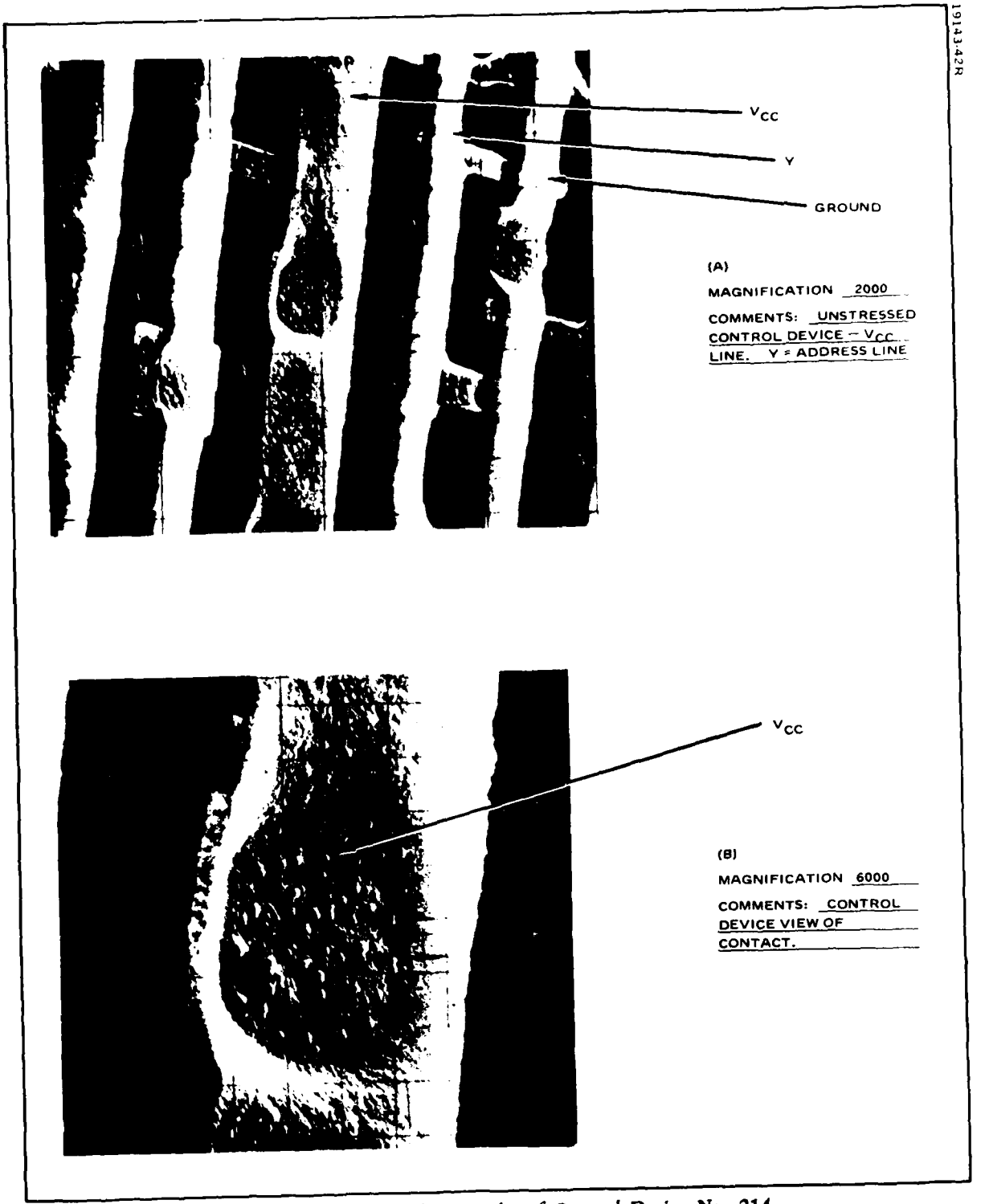


Figure B-10. SEM Photographs of Control Device No. 214

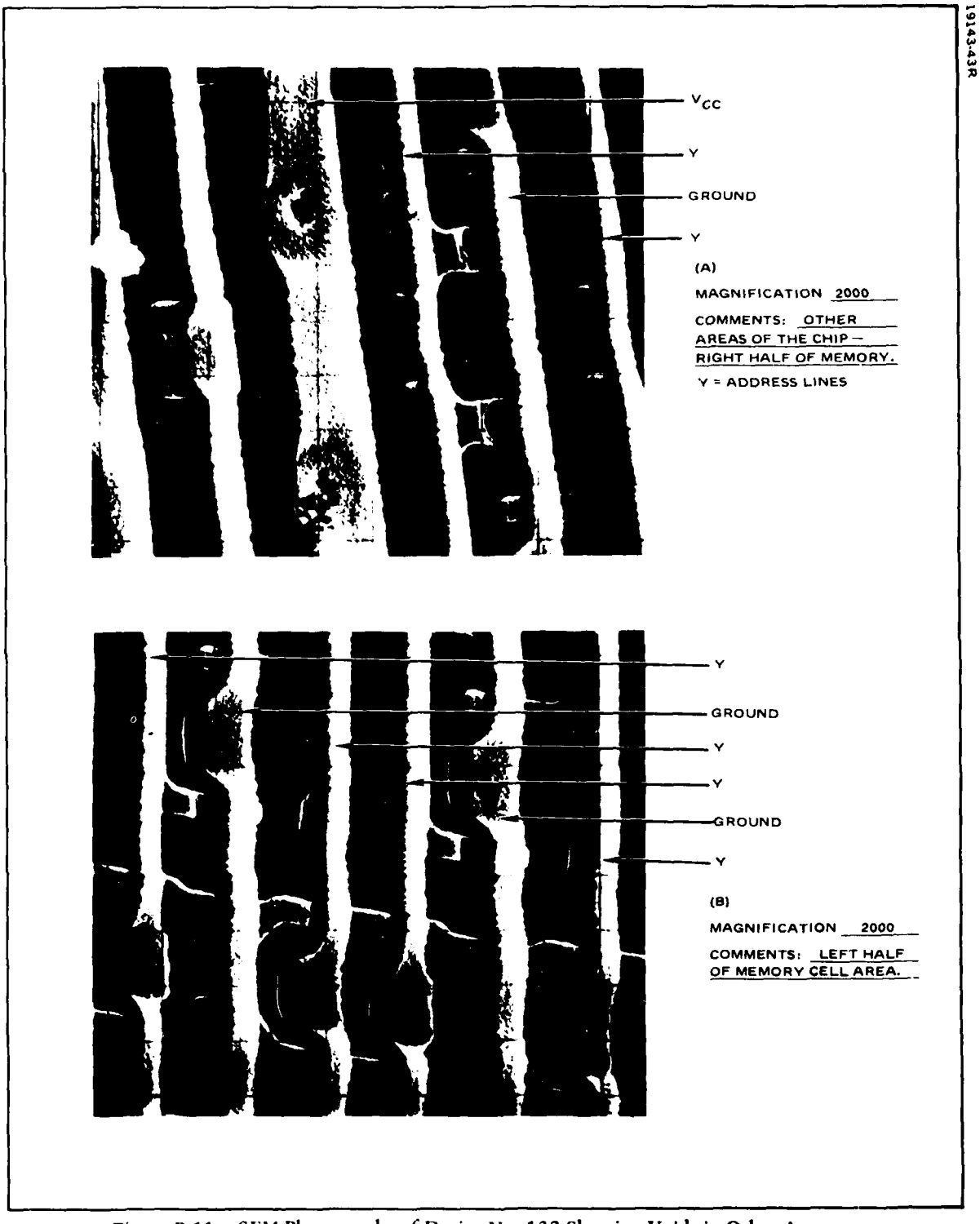


Figure B-11. SEM Photographs of Device No. 132 Showing Voids in Other Areas

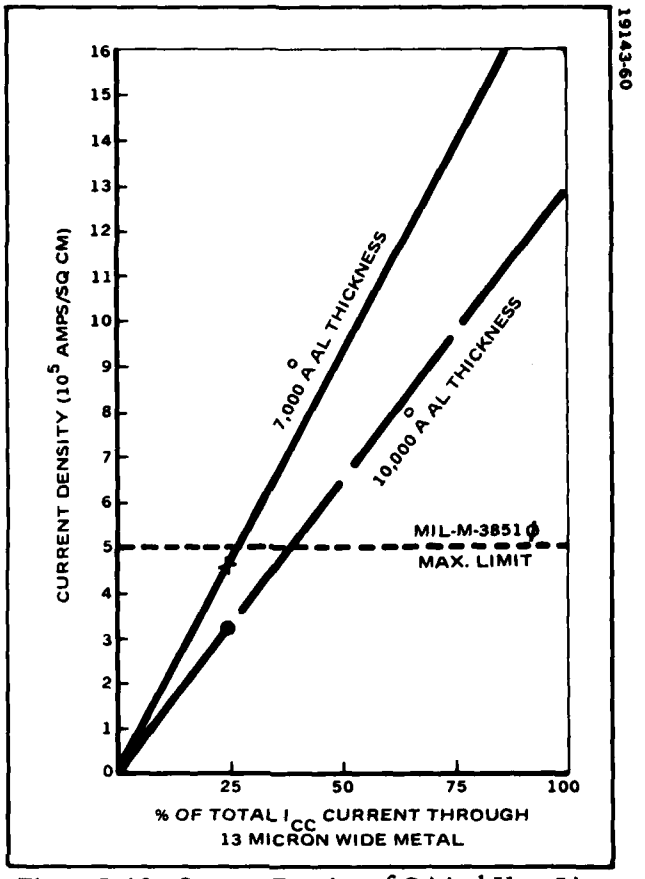


Figure B-12. Current Density of Critical $V_{CC}$ Line as a Function of 3 Other Main Branch Lines (Total $I_{CC}$ = 170 Ma Max.)

DYNAMIC RAM TESTING

It was decided that a life test should be run with the device in a dynamic condition so that the memory would be operating in known states that are under voltage or power stress (see Figure B-13). A straight static test would have the internal dynamic circuits in a non-definitive condition with the Chip Enable at either high or low. With the Chip Enable signal in a dynamic clocked condition, all internal timing circuits are traversing through two distinct operating states. The dynamic memory address driver, when the chip is in Write condition, automatically writes a "1" at all addresses. Data input is a "1" to assure that a "1" is always placed in one half of the memory and a "0" in the other half.

The 30 dynamic memories tested consisted of 15 suspect parts (short memory retention time) and 15 non-suspect parts (long memory retention time).

The accelerated dynamic life test was started on March 24, 1981. Figure B-13 shows the test conditions and block diagram for these devices. Figure B-14 shows the detail hook up of a single device. The test temperature was established at 150°C, with a test period extending to 1500 hours.

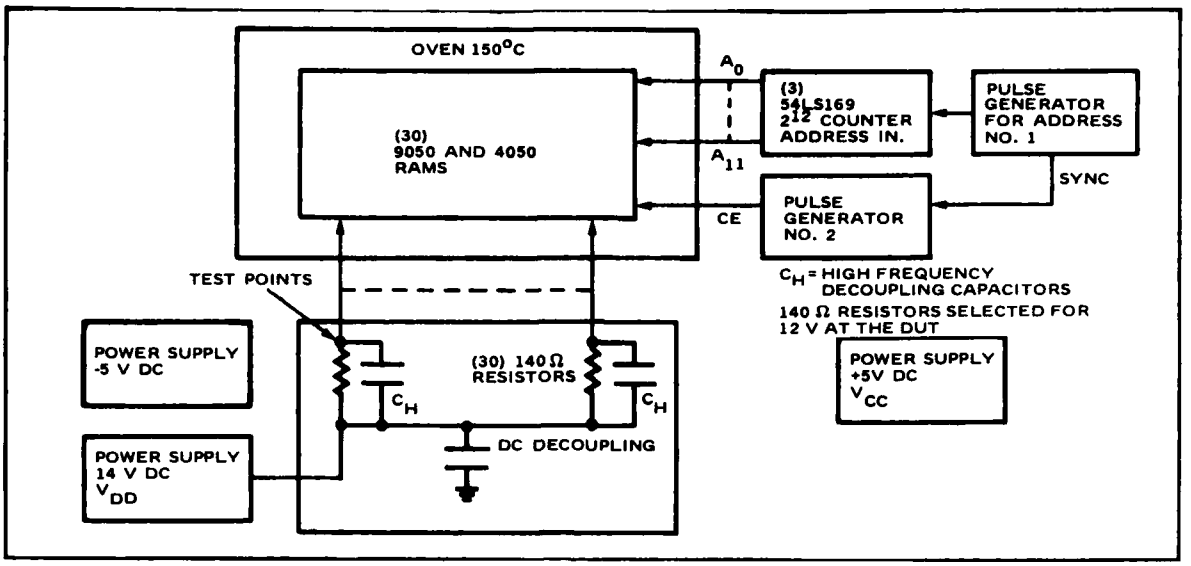


Figure B-13. Block Diagram of Life Test of Dynamic RAM

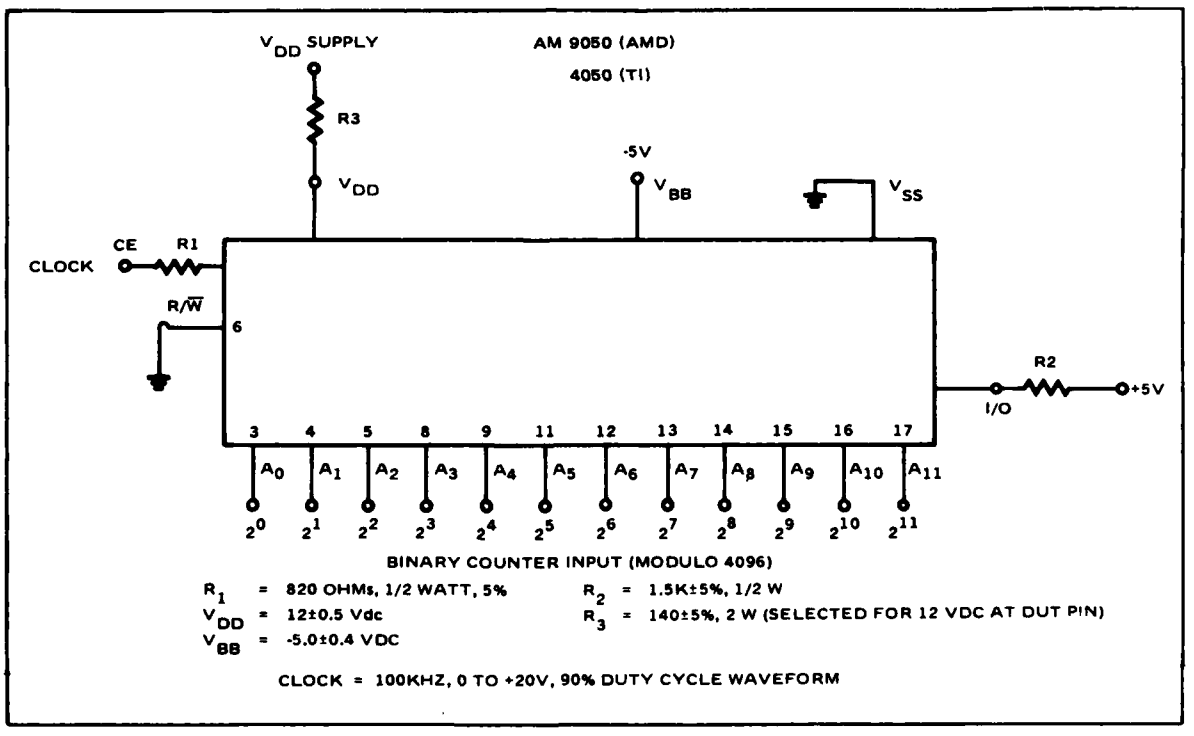


Figure B-14. Dynamic RAM Life Test Configuration

As with the static RAM testing, protective resistors were placed in the $V_{dd}$ line. Figure B-15 shows that maximum power dissipation is limited to 350 mW with a short circuit limit of 100 mA, through use of the 140-ohm resistor.

The voltage at the $V_{dd}$ pin was adjusted to a nominal of 12.0 volts by varying the $V_{dd}$ supply voltage and trimming the resistors. The voltage at the $V_{dd}$ pin ranged from 12.5 to 11.5 volts, and was monitored daily during the life test.

Data at 500 Hours of Life Test – The 500-hour life test point was reached on April 14, 1981. Table B-5 shows a failure summary as a function of selected test parameters, TWCEH, Dynamic Refresh, and V-BUMP, and $I_{dd}$. There were failures of 7 devices with no catastrophic or functional failures. All failures were the result of AC or DC parametric tests.

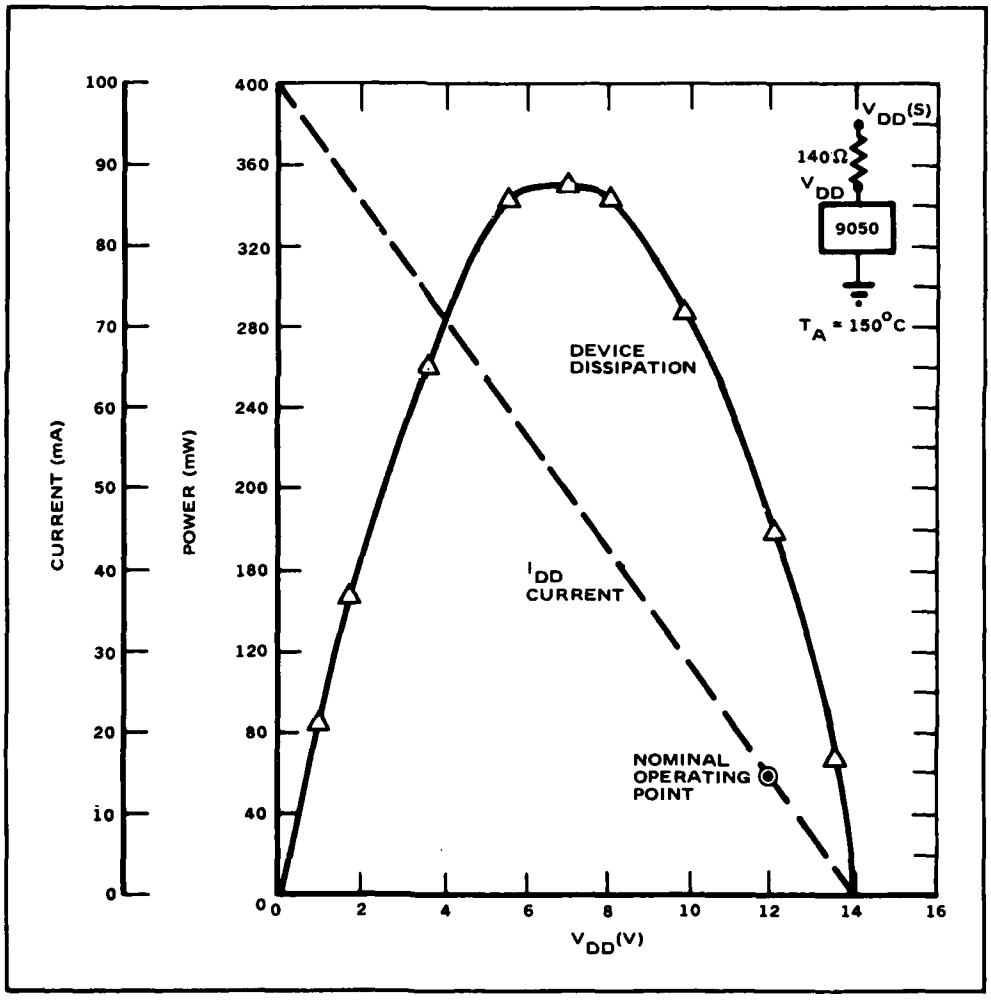


**Figure B-15. Power Dissipation of 9050 Dynamic RAM with 140-Ohm Series Resistor on $V_{DD}$**

TABLE B-5. DYNAMIC RAM FAILURE SUMMARY (500 HRS)

| 85°C | TWCEH (μs) 4.0 μs min | V-BUMP (1) | V-BUMP (0) | Refresh Start (ms) | Refresh 500 Hr (ms) | Idd |
|---|---|---|---|---|---|---|
| 134 (S) | - | F | - | 27.0 | 11.4 | |
| 206 (C) | - | F | F | 27.1 | 11.4 | |
| 220 (C) | - | F | F | 55.4 | 14.6 | |
| 227 (C) | 0.80 | F | F | 24.0 | 9.8 | |
| 229 (C) | - | - | F | 17.7 | 8.3 | |
| 260 | 1.96 | F | F | 24.0 | 6.7 | |
| 359 | 2.57 | F | F | 8.2 | 3.6 | |
| 0°C | | | | | | |
| 227 (C) | - | - | - | - | - | F |

S = Suspect
C = Control

TWCEH is tested at the maximum pulse width of the chip-enable high signal. The chip is active during this period and all the periphery dynamic circuits are writing or reading the selected memory cell. The memory is strobed during the latter part of the chip-enable pulse. The device is expected to sustain operation to the four microseconds maximum allowable chip enable high pulse width.

In the typical bootstrap dynamic circuits, shown in Figure B-16, the bootstrapped voltage node at X is typically 1.75 $V_{dd}$. Vout is driven to a Vdd level if the voltage at node X is kept above $V_{dd}$ + Vt. $V_{out}$ will lose its drive capability as the voltage at X leaks off. The voltage at X will leak off in time, since the capacitance is made up of a small junction diode and a dielectric capacitor in parallel (similar to the memory cell capacitors).

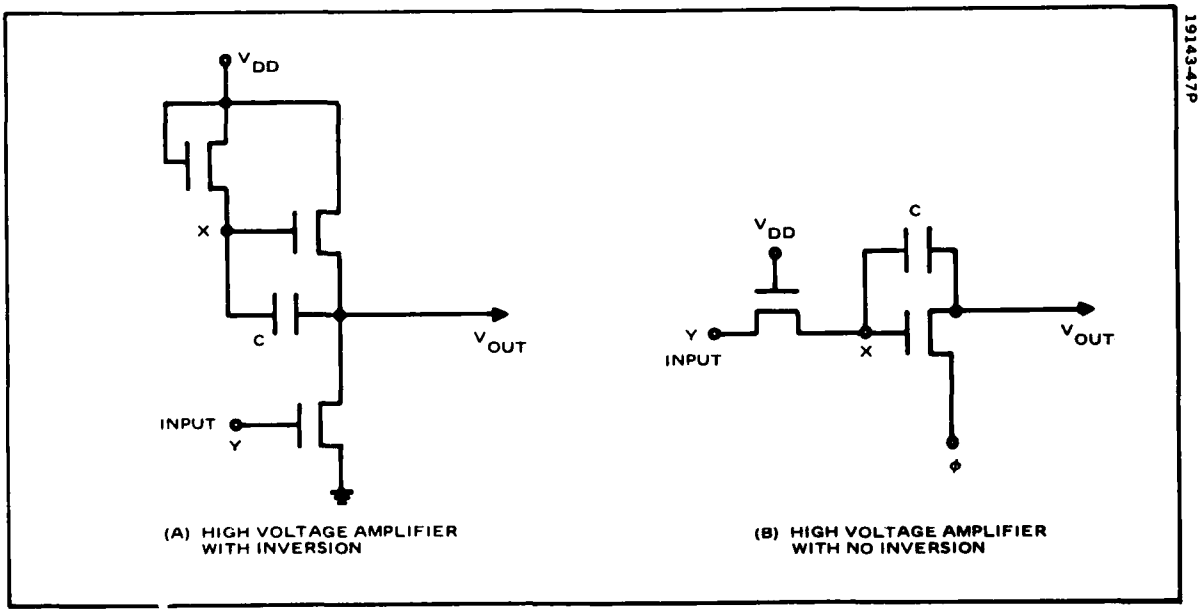


Figure B-16. MOS Dynamic Bootstrap Amplifiers

Therefore, a failure of a TWCEH test means a failure of one of the dynamic periphery circuits within the memory chip, and becomes another check of the charge storage capability. Originally, the TWCEH test was a go/no-go function, but a test program was added to determine quantitatively the maximum pulse the device can attain within the 4-microsecond test period. Thus, any deterioration of this parameter with time can now be determined.

V-BUMP has not been normally used as a test specification requirement, but many memory suppliers use it as an in-house test requirement. V-BUMP (0) is a memory test which checks for "0" cell sensitivity data by writing a "0" with minimum $V_{dd}$ (11.5V) and maximum negative $V_{bb}$ (-5.5V). The "0" cell data is read for a "1" level with $V_{dd}$ being bumped up to a higher level (+12.5V) and with a less negative $V_{bb}$ (-4.5V). Any pickup of a "1" level instead of a "0" level indicates an error. The reduction of $V_{bb}$ to -4.5V reduces the transistor threshold voltage (Reference 9), making sense amplifiers more sensitive to lower level signals. Normally an all "0" write pattern will fill the DATA half of the memory with "0" cell charges and the $\overline{DATA}$ half will have "1"s stored in the cells. The test software program was modified to allow both halves of the memory to be stored with all "0"s or all "1"s.

V-BUMP(1) is primarily a sensitivity test to write and read "1" level cells for the entire memory with worst-case $V_{dd}$ (11.5V) and $V_{bb}$ (-5.5V).

Table B-6 shows that all TI suspect devices were V-BUMP failures before the life test began. The suspect devices were selected on the basis of their short refresh times. Apparently, TI does not do a V-BUMP test, as otherwise these parts would have been rejected. Table B-6 also summarizes all dynamic memory device life test results. The most disturbing factor is that the refresh times on all the devices were significantly reduced from the values established prior to start of the life tests. An evaluation test at 1000 hours verified that the refresh time was back up to reasonable levels. Further investigation showed a temperature probe error at the 500-hour point.

Data at 1000 Hours of Life Testing – The 1000-hour life test point was reached on May 7, 1981. A review of the test data showed that the devices suffered no new failures except for those that were marginal failures prior to the start of the test. Figures B-17 and B-18 show that refresh times at 25°C and 0°C temperatures respectively are relatively consistent and do not exhibit a trend towards degradation, except for Device No. 594. This particular part was out of specification before the start of the test. Figure B-19 shows that refresh time at 85°C has come back up to a more reasonable and expected value.

Data at 1500 Hours of Life Testing – The 1500-hour life test on the dynamic RAMs was completed on June 2, 1981. No functional failures occurred during the entire 1500 hours at 150°C. Two DC parameter rejects, at 0°C, occurred when IDD maximum limits were exceeded at 1500 hours. Data on the three special test parameters being monitored were studied for any indication of significant drift characteristics or correlation to electrical parameter rejects.

A series of refresh time measurements was taken at the end of the 1500-hour life test to detect any latent temperature recovery characteristics. Initial refresh measurements at 85°C were taken within two hours of coming out of the ovens, and another set of measurements was taken four hours

TABLE B-6. DYNAMIC RAM SPECIAL TEST PARAMETER DATA SUMMARY (85°C)

| Device No. | Refresh (ms) (1 ms min) | | TWCEH (µs) (4 µs min) | | V-BUMP | | | | Supplier |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Start | | 500 Hr | | |
| | Start | 500 Hr | Start | 500 Hr | 1 | 0 | 1 | 0 | |
| 1 C | 178.0 | 42.8 | | | | | | | AMD |
| 2 C | 112.0 | 27.1 | | | | | | | AMD |
| 3 C | 140.0 | 31.8 | | | | | | | AMD |
| 4 C | 115.0 | 24.0 | | | | | | | AMD |
| 5 C | 74.0 | 22.4 | | | | | | | AMD |
| 6 C | 77.0 | 16.1 | | | | | | | AMD |
| 8 C | 112.0 | 24.0 | | | | | | | AMD |
| 9 C | 99.0 | 19.3 | | | | | | | AMD |
| 206 C | 27.1 | 11.4 | | | | | F | F | TI |
| 214 C | 127.0 | 44.4 | F | 1.07 | | | - | - | TI |
| 219 C | 64.0 | 20.8 | | | | | | | TI |
| 220 C | 55.0 | 14.6 | | | | | F | F | TI |
| 227 C | 24.0 | 9.8 | F | 0.80 | | | F | F | TI |
| 229 C | 17.7 | 8.3 | | | | | - | F | TI |
| 708 C | 49.0 | 22.4 | F | 0.88 | - | - | - | - | TI |
| 134 S | 27.0 | 11.4 | | | - | - | F | - | AMD |
| 146 S | 24.0 | 16.1 | | | | | | | AMD |
| 260 S | 24.0 | 6.7 | - | 1.96 | F | F | F | F | TI |
| 263 S | 8.28 | 3.6 | | | F | F | F | F | TI |
| 348 S | 9.85 | 5.1 | F | 0.85 | F | F | F | F | TI |
| 359 S | 8.28 | 3.6 | - | 2.57 | F | - | F | F | TI |
| 435 S | 6.71 | 3.6 | - | 3.8 | F | F | F | F | TI |
| 470 S | 8.28 | 3.6 | | | F | F | F | F | TI |
| 480 S | 6.71 | 3.6 | F | 0.66 | F | F | F | F | TI |
| 493 S | 6.71 | 3.6 | F | 0.94 | F | F | F | F | TI |
| 520 S | 14.58 | 6.7 | | | F | - | F | F | TI |
| 594 S | 1.66 | 0.7 | F | 1.62 | F | F | F | F | TI |
| 627 S | 13.0 | 6.7 | F | 0.56 | F | F | F | F | TI |
| 659 S | 14.58 | 5.1 | F | 0.44 | F | F | F | F | TI |
| 821 S | 8.28 | 3.6 | | | F | F | F | F | TI |

C = Control (non-suspect)
S = Suspect

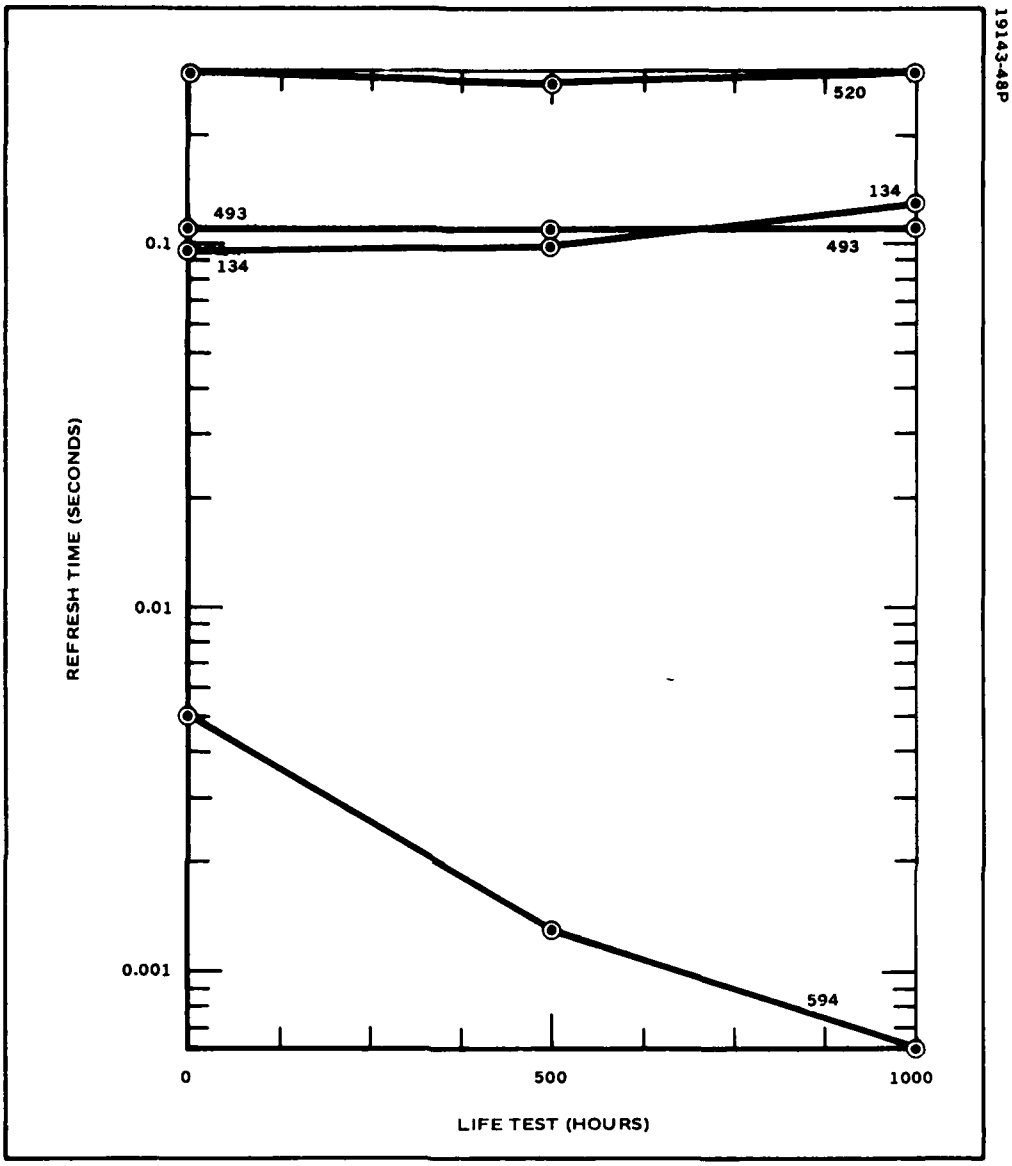


Figure B-17. 25°C Refresh Time

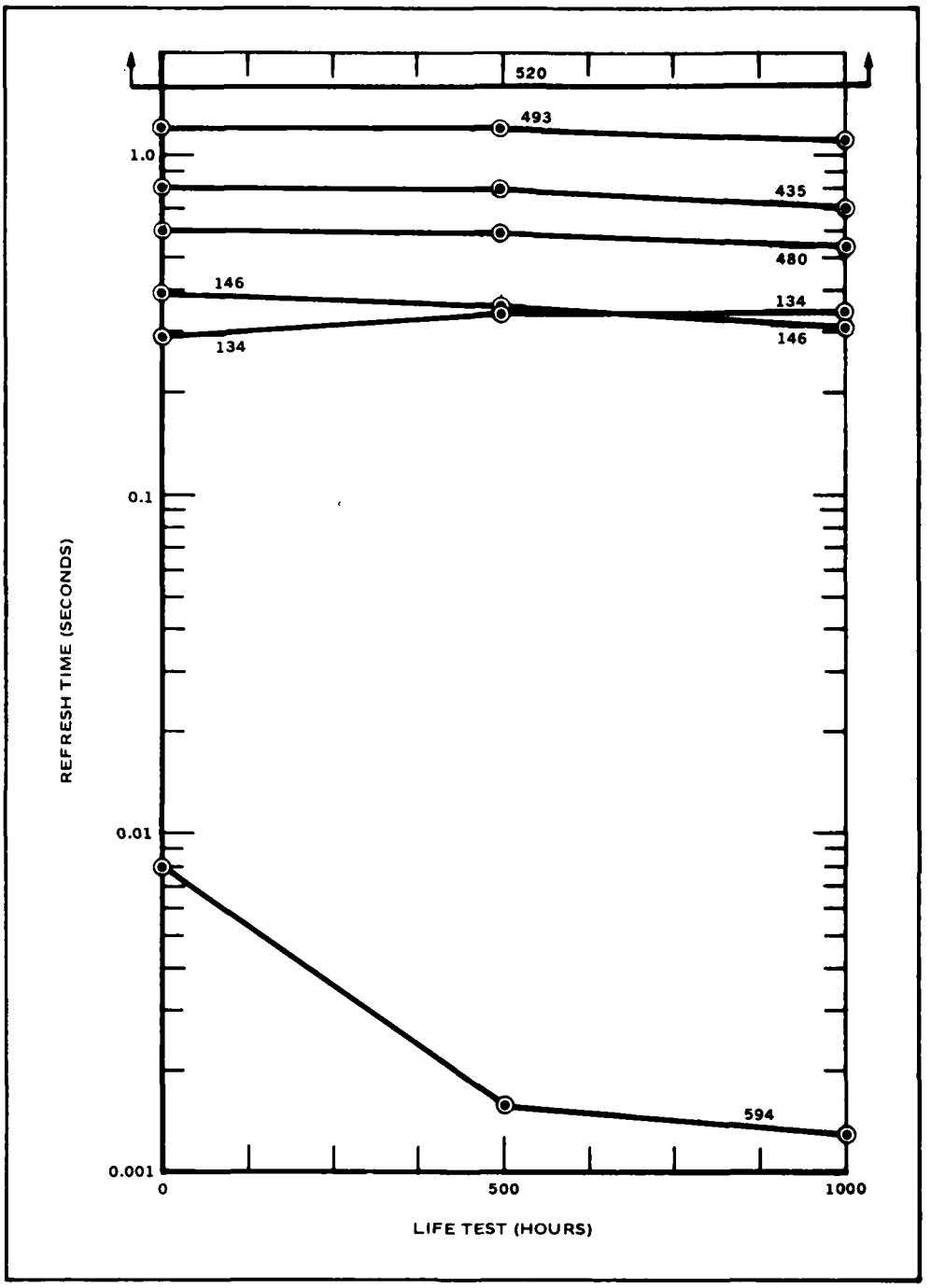


Figure B-18. 0° Refresh Time

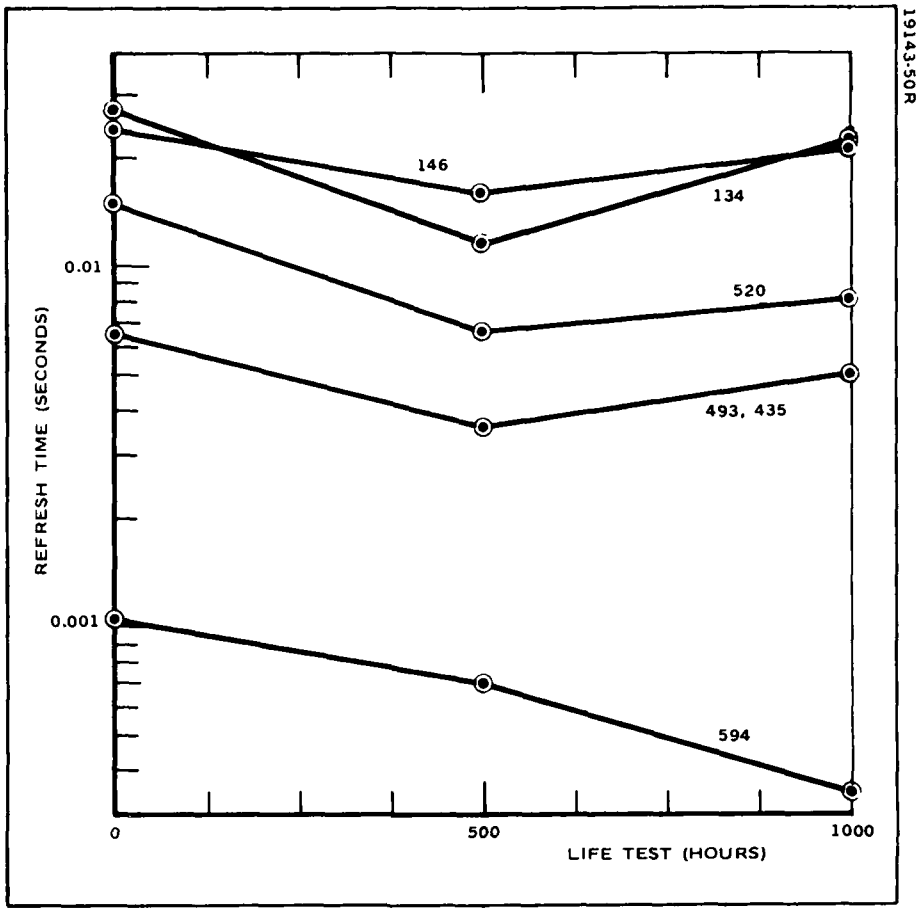


Figure B-19. 85°C Refresh Time

later. The second set of readings was consistent with the original readings, thus dispelling any concern over device thermal instability and recovery time requirements. Figures B-20 and B-21 show that the average refresh times at the 1500-hour point were consistent with readings taken at 0 and 1000 hours. However, readings at 500 hours were all consistently low.

A thorough investigation and review of temperature testing procedures and measurements indicated that a problem existed with one of the two portable Thermo Stream environmental temperature control systems utilized for checking semiconductor IC devices. One of the units was determined to have been out of calibration during the period of the 500-hour measurements. A thermocouple is normally in the middle of the gas flow stream, holding the gas temperature to a constant preset value. It was discovered that the thermocouple was actually off to one side where it was relatively cooler. Being in a closed loop heat control system, the heating unit was subjecting the devices to higher temperatures than indicated. This resulted in measuring shorter refresh times for the devices, since the device leakage was higher.

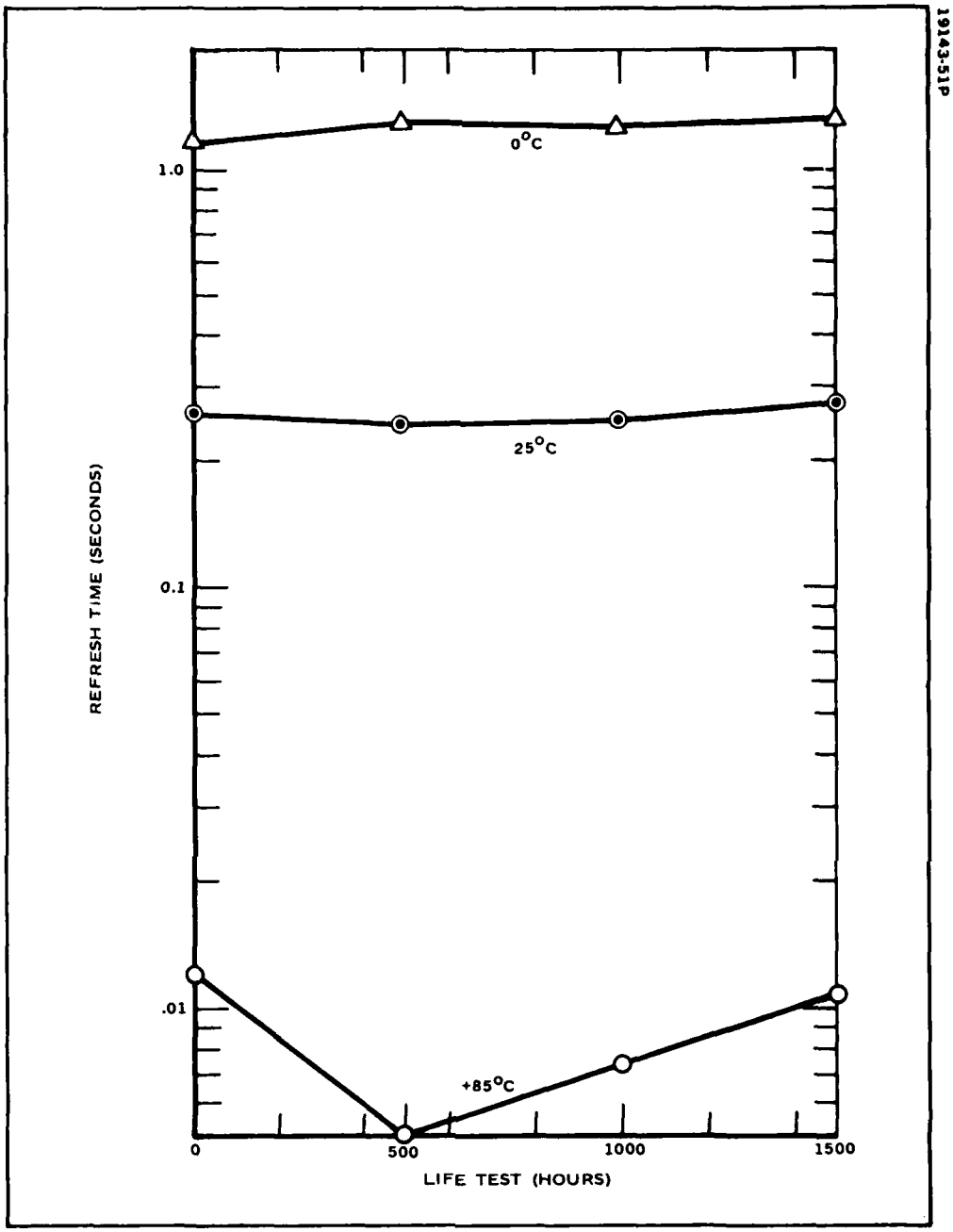


Figure B-20. 9050, 4050 Dynamic RAMs Average Refresh Time – Suspect Parts

TWCE and V-BUMP results for the 1500 hour point are summarized in the main text. TWCE data indicated relative stability with life testing to 1500 hours. V-BUMP is a go-no-go test only, so that quantitative results are not given for this test parameter. However, the total number of failures were monitored and no increases were noted.

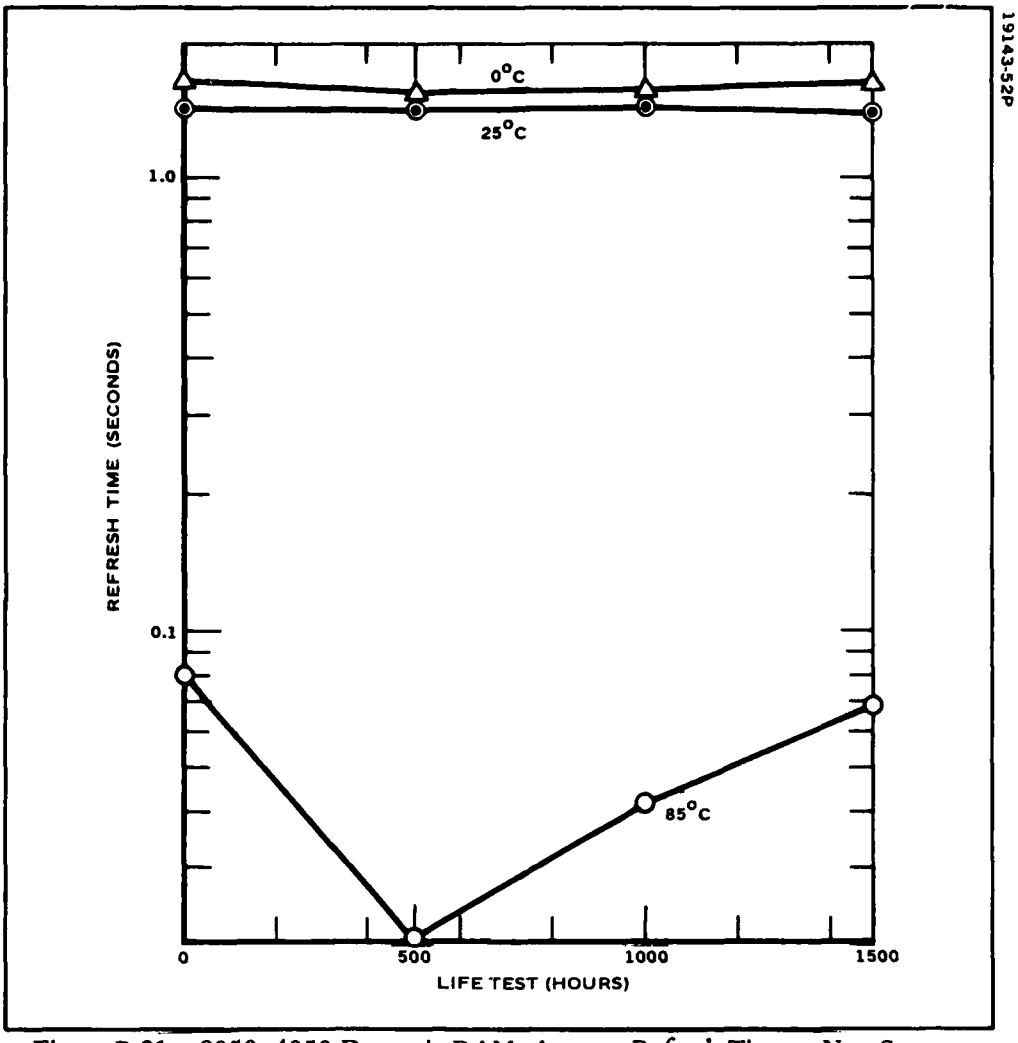


Figure B-21. 9050, 4050 Dynamic RAMs Average Refresh Time – Non-Suspect Parts

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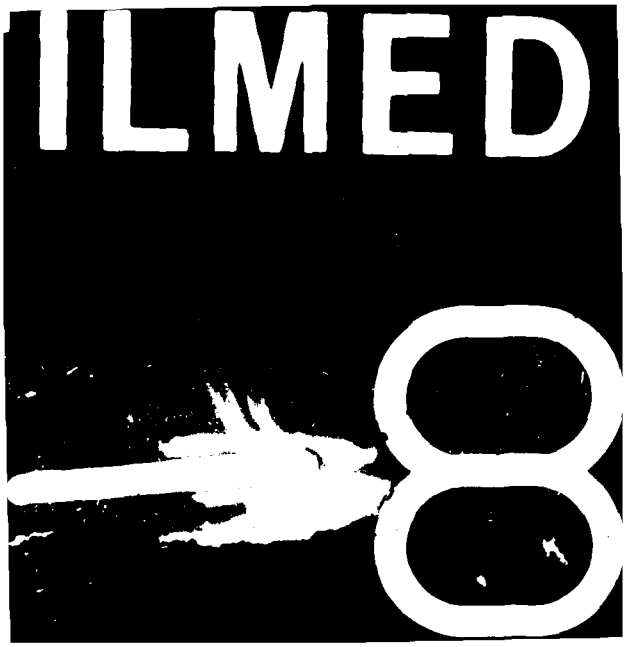
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8